Farnell

Instructions/Service Manual for PSG1000

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CONTENTS

1. SCHEDULE OF EQUIPMENT

The instrument has been carefully packed to prevent damage in transit. When removing the unit from the packing box, ensure that all parts and accessories are removed from the packing material. Retain the packing box and material.

The complete equipment comprises:

1 off Farnell PSG1000 Signal Generator

1 off detachable a.c. power lead

1 off type N to BNC adapter

1 off BNC to BNC coaxial cable

1 off Instruction/Service manual

1 off three pin d.c. input plug

1 off six way auxiliary connection plug and loom.

Note: In the event of damage in transit or shortage in delivery separate notices in writing should be given to both carriers and Farnell Instruments Limited, or local agent if outside the UK, within three days of receipt of the goods, followed by a complete claim within five days. All goods which are the subject of any claim for damage in transit or missing items should be preserved intact as delivered, for a period of seven days after making the claim, pending inspection or instructions from Farnell Instruments Limited, or an agent of this company.

2. INTRODUCTION

The PSG1000 is a field portable Signal Generator featuring direct RF synthesis to 1GHz and a full +13 to -133dBm output level range. The generator operates from a.c. or d.c. power sources.

Front panel controls are of the touch sensitive membrane type which gives superior reliability to conventional switches and allows a flat front panel completely sealed against the ingress of moisture and dust. Acoustic and tactile feedback is provided, with each key having an embossed area to aid location. A hidden layer of metal foil in the front panel ensures R.F. leakage is negligible. The front panel includes LED displays of carrier frequency and carrier level or modulation rate and modulation level. An analogue meter is also included for displaying SINAD signal to noise ratios, the external modulation level or the battery state when d.c. power is applied. Data may be set using the keypad by first touching the required numbers and then a Unit key. The entered data is displayed in the data entry window as it is entered.

All erroneous entries or impossible requests made on the microprocessor result in an audible warning and the ignoring of the command. Partially entered data may be cleared without execution if desired.

Updating of parameters may be accomplished by a set of four keys. Two of the keys allow a cursor to be moved over any one of the displayed digits. This digit can then be incremented by the remaining up/down keys.

In addition to the integer incrementation of displayed data the delta key allows data to be changed in steps of any resolvable size. The steps are preset using the keypad and the required digit may by incremented in the set step size by the up/down keys.

Automatic conversion calculations are performed by the microprocessor enabling carrier levels to be entered and displayed in the various units of db, Volts, e.m.f. and p.d.

The entire parameters of the last used front panel settings will be automatically retained in non-volatile memory following a power break. In addition, one hundred entire front panel set ups may be stored in non-volatile memory and recalled at a later date.

Extra features include a shifted function key to enable standard and special facilities to be accessed. Digital sweep of displayed data is also permissible, with the ability to set start, stop points and the total sweep time.

A built-in fast locking modulation synthesizer gives more versatility than the usual spot frequencies and enables precise continuous tones to be set up for CTCSS systems, sequential tones to be programmed for SELCALL systems and modulation bandwidth to be accurately checked. Also included is a single extra 1kHz tone of low distortion. This can be used independently of the synthesized oscillator or simultaneously to enable two tone tests to be performed. External modulation sources may be used either independently or mixed with the internal synthesized oscillator. Additionally the external modulation level is displayed on the front panel analogue meter to enable the modulation to be calibrated. Adjustment of external level is also provided with the external level control.

The wide modulation bandwidth extends down to d.c. to cater for low rate data streams. Phase modulation as well as a.m. and f.m. is a standard feature.

An internal 1kHz distortion analyser is also incorporated to enable SINAD sensitivity tests to be performed on mobile radios.

Other standard features include IEEE 488 programming and reverse power protection.

3. SPECIFICATION

FREQUENCY

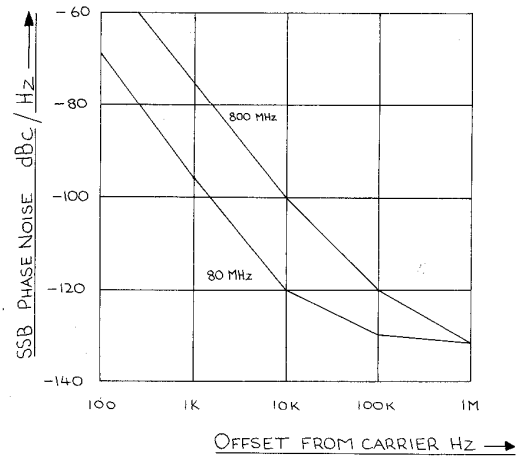
Range	10kHz to 1000MHz
Resolution	10Hz (<128MHZ) 100Hz (≥ 128MHz)
Lock Speed (to 100Hz)	<500ms
Accuracy	± $5E^{-8}$ ex-factory, 20°C
Stability	± $1E^{-6}$ (0 to + 55°C) ± $2E^{-7}$ per month

RF OUTPUT

Range	-133dBm to +13dBm (0.05µV to 1V p.d.)
Resolution	0.1dB
Units	dBm, dBµV, mV, pd, emf
Accuracy	± 1dBm at +13dBm ± 1.5dB overall (<500MHz) ± 2.5dB overall (≥500MHz)
Source impedance	50 Ω
VSWR	<1.5:1 (-3dBm)
Reverse Power Protection	50W max. d.c. to 1GHz (user reset)
Trip level	200mW typical

SPECTRAL PURITY

Harmonics	<-25dBc (carrier < +7dBm)
Sub harmonics	None
Non harmonic spurious	<-60dBc
Residual FM	<50Hz r.m.s. at 1GHz (CCITT P53A weighting) improving 6dB/octave to <1.5Hz r.m.s. at 16MHz <6Hz r.m.s. below 16MHz
Residual AM	<0.1% (50Hz to 15kHz bandwidth)
SSB noise	Typical characteristics shown for carrier frequencies of 80 and 800MHz



Noise Floor	<-130dBc
AM on 20kHz FM	< 0.5% (50Hz to 15kHz bandwidth), 1kHz rate
FM on 30% AM	<200Hz (50Hz to 15kHz bandwidth), 1kHz rate
Carrier leakage	< 0.5µV (2 turn 2mm loop, 25mm away)

AMPLITUDE MODULATION

Depth	0 to 99.9% (< 500MHz <+7dBm) 0 to 50% (≥500MHz <+7dBm)
Resolution	0.1%
Accuracy	± 5% of reading (<90% depth)
Bandwidth (1dB)	d.c./10Hz to 25kHz
Distortion	<2% at 50% depth, 1kHz rate <5% at 80% depth, full bandwidth

FREQUENCY MODULATION

Maximum peak deviation	10kHz to <16MHz, 100kHz 16MHz to <32MHz, 25kHz 32MHz to <64MHz, 50kHz 64MHz to <128MHz, 100kHz 128MHz to <256MHz, 200kHz 256MHz to <512MHz, 400kHz 512MHz to 1000MHz, 800kHz
Resolution	Carrier frequency ≥64MHz 10Hz (<10kHz peak) 100Hz (10 to <100kHz peak) 200Hz (100 to <200kHz peak) 400Hz (200 to <400kHz peak) 800Hz (400 to 800kHz peak) Carrier frequency <64MHz 10Hz (<10% maximum peak deviation) 100Hz (≥10% maximum peak deviation)
Accuracy	± 5% of reading

Bandwidth (1dB)	d.c./50Hz to 25kHz
Distortion	< 1% <10kHz deviation, 1kHz rate < 5% <100kHz deviation, full bandwidth

PHASE MODULATION

Deviation	0 to 3 rads
Resolution	0.01 rad
Accuracy	± 10% of reading
Bandwidth (1dB)	50Hz to 10kHz
Distortion	< 2% at 1kHz rate

INTERNAL MODULATION SOURCES

Synthesizer range	10Hz to 9.999kHz
Resolution	0.1Hz <1kHz 1Hz ≥1kHz
Lock Speed	< 5ms
Accuracy	± $2E^{-5}$
Distortion	< 2% < 5kHz
Synthesizer output	0 to 1V r.m.s. (emf 50Ω) in 1mV steps
Single spot frequency	1kHz

Accuracy	$\pm$ 2E^{-5}
Distortion	< 0.2%
Simultaneous tones	Ratio fixed tone to variable tone 5:1
Internal 1kHz output	1V r.m.s. (emf 50Ω)
SEQUENTIAL TONES	
Systems covered	CCIR, EEA, ZVEI-1, ZVEI-2, EIA, NATEL
EXTERNAL MODULATION	
Impedance	50kΩ
Level	1V r.m.s. for f.s.d. (front panel adjustment control for higher levels)
Indication	Analogue meter (scaled 0 to 1 with "CAL" marker)
Simultaneous tones	The external input may be mixed with the internal synthesizer. Ratio of external tone to internal tone 5:1
SINAD	
Input frequency	1kHz
Input level	30mV to 3V r.m.s.
Indication	Analogue meter, scale range 30db to 6db
Impedance	> 5kΩ
Bandwidth (3dB)	60Hz to 6kHz

SWEEP

Functions	Carrier frequency, carrier level, modulation frequency, modulation level
Range (start, stop)	Any within setting range
Total sweep time	2 seconds to 200 seconds

GENERAL

Programmability	IEEE 488 and HP-IL (option)
Memory (non volatile)	100 complete front panel set ups. Last front panel set up. IEEE 488 address
Internal crystal reference	TCXO, 10MHz
Internal reference output	3V pk-pk (emf 50Ω)
External reference frequency	10MHz
External reference level	1V r.m.s.

POWER REQUIREMENT

Voltage	100, 120, 220, 240V (48 to 440Hz a.c.)
Tolerance	± 10%
D.C. input	11.5 to 15V or 23 to 30V (factory option)
Consumption	30VA maximum

ENVIRONMENTAL

Temperature (operating)	0 to + 50°C
(storage)	-40 to + 70°C
Relative Humidity	95% to 40°C non condensing
Vibration	5 to 150Hz 2G sinusoidal 15 minutes in each of 3 orthogonal planes
Shock	10 off 25mm drops on each of 6 faces
Safety	Designed to comply with BS4743/IEC348
RFI emission	Complies with BS800/EEC 76/889

MECHANICAL

Height (including feet)	145mm
Width	330mm
Depth	405mm
Weight	8.6kg

PULSE MODULATION OPTION

Frequency range	25MHz to 1000MHz
Carrier on/off ratio	60dB at 70MHz 45dB at 500MHz 40dB at 800MHz
Pulse rise time	2µs
Pulse fall time	1µs

Minimum pulse width	4µs
Modulator insertion loss	< 4.5dB
TTL logic drive (Maximum 5V peak)	TTL High = Carrier on TTL Low = Carrier off
Carrier leakage	< 0.5µV (2 turn 25mm loop, 25mm away) carrier level < -3dBm

4. INSTALLATION

4.1 INITIAL SETTING UP - A.C. SOURCE

Check the power input setting is correct for the local supply by looking through the clear window adjacent to the power input socket on the rear panel. One of four alternative settings will be visible. Should it be necessary to change the setting, slide the window across, remove the fuse and then pull out the small selector card using the puller provided. Re-insert the card in the appropriate alternative position so that the required voltage setting is visible when the card is fully replaced. Replace the fuse ensuring the rating is correct for the voltage to be used, and slide the window across.

Connect a suitable plug to the power cable observing the following colour code:

Live - Brown

Neutral - Blue

Earth - Green/Yellow

Plug power cable into socket on rear of instrument and power source. Switch on using the power switch on the rear of the instrument.

4.2 D.C. SOURCE

Apply a d.c. input via the three pin connector on the rear panel by correctly wiring the three plug supplied as part of the accessory package. The connections are as follows:

Pin 1 - Instrument chassis earth

Pin 2 - D.C. Negative

Pin 3 - D.C. Positive

The d.c. supply must be within the range 11.5 to 15V (or 23 to 30V for the +24V d.c. option) with a current capability of 2 amps. Switch on using the power switch on the rear of the instrument. The instrument is fully protected against accidental d.c. polarity reversal.

4.3 RACK MOUNTING

The instrument may be mounted in a standard nineteen inch rack using the kit available as an optional accessory (order code 17PSG1000E).

For rack mounting applications the unit's support feet (located on the lower cover) must be removed as follows:

Place the instrument with the lower cover facing upwards and hinge forward the front tilt feet. Remove the eight screws (four each side) securing the feet support bars to the lower cover and remove the support bars complete with feet. Retain the screws and support bars for future use.

To fit the rack mounting "ears", carefully prise out the insert in the outer face of both front handles (retain for future use). Fit each ear into the exposed recess, securing with the M4 x 10 CSK screws provided. It is important to ensure that some provision be made to support the rear of the unit when using the rack mounting ears.

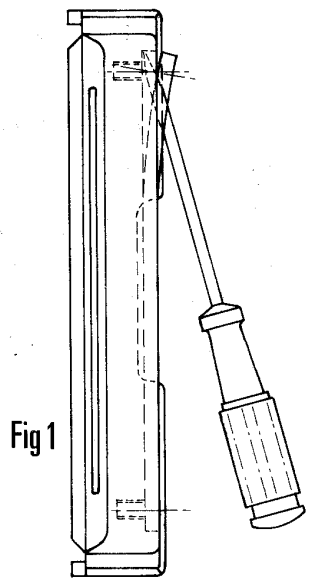


Fig 1

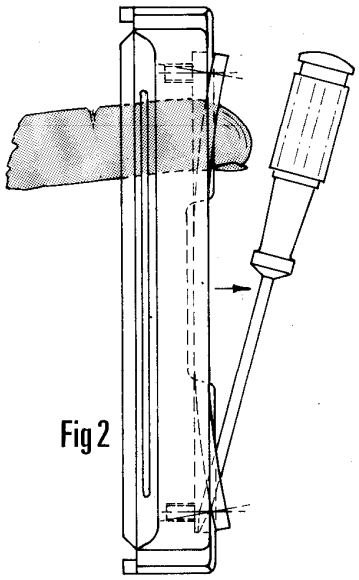


Fig 2

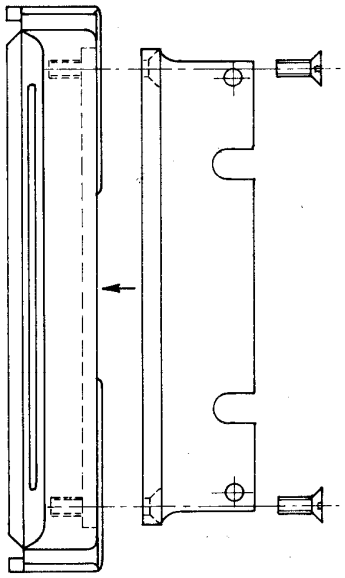


Fig 3

PROCEDURE FOR ATTACHMENT OF RACK MOUNTING BRACKET

REF. FIG 1
Insert small screwdriver into thin gap between insert and handle body. Prise away one end slightly and hold in position with finger.
Note orientation of insert with styling cut-out opposite cut-out in handle.

REF. FIG 2
Insert screwdriver into other end and repeat procedure. This will relieve the small tapered pins of the insert from the threaded holes in the handle. Remove insert in direction of arrow.

REF. FIG 3
Insert rack mounting bracket into recess in handle in attitude shown and secure firmly with 4 M4 x 10LG C'SK HD screws supplied.

5. OPERATING INSTRUCTIONS

5.1 DISPLAY AND DATA ENTRY

a) The PSG1000 has two fundamental display modes, either display carrier functions (DISP CARR) or display modulation functions (DISP MOD).

Data entry can be made in either mode, but to alter carrier frequency or carrier level the DISP CARR mode must be selected.

If an invalid key selection is chosen, IGNORED appears momentarily in the data entry display.

The display mode can be changed during data entry and if required the CLEAR key abandons data entry mode.

Additionally the key functions listed below operate independently of the selected display mode:

RF OFF, INT 1kHz, EXT MOD, SYNTH RATE, MOD OFF and DCFM.

b) Data entry is performed by first entering the numeric data followed by a terminating function key. In response to data entry the PSG1000 replaces the previous contents of the eight digit display with the contents of the data entry buffer. The buffer will accept a maximum of 64 characters but only the last 8 are displayed. A prompt line is provided to annunciate the data entry mode. Also the displayed data entered may be edited by utilising the cursor position keys ← → to remove entered data or provide a space.

If the entered value is invalid for the specification limits of the instrument an error code is momentarily displayed in the four digit display.

5.2 CARRIER FUNCTIONS

a) Select the DISP CARR mode and enter data for the required carrier frequency. A choice of three terminating keys is provided, GHz, MHz, or kHz. For frequencies less than 128MHz the displayed resolution is 10Hz, and 100Hz above.

b) Proceed with entered data for the carrier level, terminating with one of the six possible function keys dBm, dBμV, mV, μV, pd or emf.

Full carrier level units conversion is provided so that outside of the data entry mode, selecting alternative units will update the carrier level display.

The instrument is protected against excessive RF power accidentally applied to the output connector. When an excessive voltage is detected the RF output is disconnected, RF OFF automatically selected and a warning message displayed together with an audible bleep. When the overload voltage is removed, the RF output remains disconnected until RF OFF is deselected.

Additionally RF OFF may be selected or deselected at any time.

5.3 MODULATION SOURCES

a) The available modulation source possibilities are internal 1kHz fixed frequency, internal audio synthesizer (10Hz to 9.999kHz) or external audio (to 25kHz).

These are displayed in the eight digit modulation rate window. The left hand half of the window shows "Int" or "Etn" when INT 1kHz or EXT MOD are selected. The last four digits display the audio synthesizer rate in kHz when SYNTH RATE is selected.

To alter the synthesizer rate simply key in the new frequency terminated with the kHz key. In the range 0.010kHz to 0.999kHz the displayed resolution is 1Hz, with a setting resolution of 0.1Hz.

Any of the three sources may be independently selected and the internal audio synthesizer can be mixed with either the 1kHz fixed tone or an external tone, but not both together. This allows complex dual tone modulation signals to be generated.

When the internal audio synthesizer is mixed with the internal 1kHz or an external source it's amplitude is reduced to a nominal 20% of the main tone.

b) When INT 1kHz is selected the front panel analogue meter is automatically switched to read SINAD. When a 1kHz audio signal within the level range 30mV to 3V r.m.s. is applied to the SINAD input the analogue meter indicates the dB SINAD ratio, scaled 30dB to 6dB.

5.4 MODULATION LEVEL

a) For modulation level the three possible terminating keys are % AM, kHz FM and RAD PM. The resulting level is displayed in the four digit modulation level window.

For % AM the displayed resolution is 0.1%, and 0.01 radian for RAD PM.

With kHz FM the resolution varies depending upon the carrier frequency and the modulation level (see specification).

b) The modulation circuits may be d.c. coupled with % AM, kHz FM by selecting DCFM.

In the % AM mode the isolating capacitor in the modulation input path is shorted out so that all the modulation paths are d.c. coupled.

When selected with kHz FM or RAD PM the synthesizer loop integrater is held at the last tuning voltage thus disabling the correction loop. The unlocked carrier can now be frequency modulated with a d.c. voltage at the modulation input.

By selecting MOD OFF the modulation signal is isolated from the carrier circuits thus removing the modulation. Additionally, MOD OFF deselects DC FM (if selected), permitting re-locking of the carrier.

5.5 STORE AND RECALL

a) The instrument will store up to 100 complete front panel settings in non volatile memory. These are designated store 00 through to store 99. Store 00 is reserved for the current front panel setting.

To store a setting, select STORE followed by the required two digit store number. Conversely, to recall a setting select RECALL followed by the store number. Recalling a setting does not change the current display mode.

If an invalid value is found during recall of any of the stores it is replaced with fixed default values of 100MHz, 0.0dBm, INT 1kHz modulation rate and 0.00 RAD PM.

b) Additionally, selective stored settings may be write protected by selecting the store number followed by#91.

The store number followed by#90 removes the write protection.

5.6 CURSOR CONTROL

a) In display carrier or display modulation modes any of the displayed digits may be incremented or decremented in consecutive steps. First select CURSOR: one of the displayed digits will now start blinking indicating the cursor position. Reposition the cursor over the required digit using the left/right keys, then alter the digit using the up/down keys.

b) The displayed digits may also be incremented or decremented in fixed steps by utilising the delta key.

Select CURSOR and position over the parameter to be varied, then deselect CURSOR. Enter the required step size, followed by DELTA, then the required units terminating key.

Operation of the up/down keys will now enable the desired parameter to be altered in the preset step size.

c) By utilising a second function, the instrument may be set in the autocursor mode. To set this mode, enter 1#77. When the desired digit is then altered by holding down the up/down key, the stepping continues when the key is released. The stepping will cease after any other key depression or if an error boundary is reached.

To stop the auto cursor mode, select#77.

5.7 SWEEP

a) In display carrier or display modulation modes the displayed values may be swept between predefined limits.

The sweep start values are entered in store 01 and the final value in store 02.

The value to be swept is identified by placing the cursor over the required parameter.

Enter a total sweep duration (valid range 2 secs to 200 secs) then terminate with the SWEEP SECS key.

Pressing the SWEEP SECS key again initiates the sweep. The sweep mode may be terminated at any point by de-selecting SWEEP SECS. Conversely, re-selecting SWEEP SECS re-enters the sweep mode.

For carrier frequency the sweep steps are executed at the rate of 6 steps/second and 10 steps/second for other functions.

5.8 ATTENUATOR LEVEL GLITCHES

a) The instruments RF level setting is obtained by a combination of 10dB fixed step attenuators switched in by relays and 0.1dB steps obtained from the output AGC loop.

At the attenuator change points of -3.0dBm, -13dBm ---- -113.0dBm the RF output is momentarily undefined for a period of approximately 3ms as the relays change over.

To eliminate this level glitch it is possible to extend the normal range of the AGC loop as below.

b) Place the cursor over the 0.1dBm level digit and commence decrementing the display. At the next attenuator change point, "Fine AGC" will be displayed in the data entry window and the RF level will continue reducing with no level glitch. When the limit of the extended AGC range is reached the message "Fine AGC" will be removed and the instrument reverts to normal attenuator settings.

The CLEAR key will exit the "Fine AGC" mode as will any attempt to change the level other than in 0.1dBm steps.

5.9 SELECTIVE CALLING TONE GENERATION

a) The instruments internal audio synthesizer produces high accuracy sine waves and is specially designed to rapidly change it's set frequency on demand, with minimum settling time. This feature is essential for selcall generation.

The software is designed to recognise the standard 5 tone systems currently in use and can cope with the 6 different systems of CCIR, EEA, ZVEI-1, ZVEI-2, EIA and NATEL.

b) To enter the selcall mode, deselect MOD OFF and select the required modulation rate and level.

Enter the five tone numbers required then## followed by a 2 digit system code, listed below:

80 for CCIR, 81 for EEA
82 for ZVEI-1, 83 for ZVEI-2
84 for EIA, 85 for NATEL.

The message "tones" appears in the data entry window followed by a blip as the selcall tones are generated.

If desired enter#88 to repeat the tone sequence once and#89 for continuous repeat.

NB. It is not possible to store a tone sequence.

5.10 ERROR CODES

Abbreviations used:

CF = Carrier frequency, CL = Carrier level
MF = Modulation frequency, ML = Modulation level.

ERROR CODE	PROBLEM
08	Bus address out of range (0-30 valid)
10	CF out of range
11	CF delta out of range
12	Store is write protected
13	Cannot store a setting with relaxed specs
14	Store number out of range
20	CL out of range
21	CL delta out of range
22	Cannot enter a delta linear CL
30	MF out of range
31	MF delta out of range
40	ML out of range
41	ML delta out of range
42	FM too high for current CF range
43	Setting AM with CL above +6.9dBm
44	Setting AM >50% with >500MHz
60	Gate function not implemented
61	Swept limit in store 01 invalid
62	Swept limit in store 02 invalid
63	Sweep secs out of range
45	Incrementing CF with DCFM selected

64	Cursor not on swept parameter
65	Swept limits too close together or sweep period too long
80	Selcall sequence should be preceded by deselecting MOD OFF
81	Selcall code sequence incorrect
82	No previous selcall code since switch on
99	Function not implemented.

5.11 NOTE CODES

51 - AM temporarily set to zero while carrier level > + 6.9dBm.
52 - FM returned to full set value after ERROR code 42.

5.12 GATE FUNCTIONS

#00	Software revision number
#11	Display test (next key exits the routine)
#22	Relax error limits (2)
#33	Bleeper on (1) (2)
1#33	Bleeper off (2)
#44	Last error code
#55	Display GPIB address
NN#55	Enter GPIB address (0-30 valid)
#66	Select internal reference frequency
1#66	Select external reference frequency
#77	Deselects auto increment mode (1) (2)
1#77	Select auto increment mode (2)
NNNNN#80	CCIR tone sequence (100ms) (2)
NNNNN#81	EEA tone sequence (40ms) (2)
NNNNN#82	ZVEI-1 tone sequence (70ms) (2)
NNNNN#83	ZVEI-2 tone sequence (70ms) (2)
NNNNN#84	EIA tone sequence (30ms) (2)
NNNNN#85	NATEL tone sequence (70ms) (2)

# 88	Repeat previous tone sequence (2) (3)
#89	Continuous repeat of tone sequence (2)
NN#90	Remove write protection of store NN
NN#91	Write protect store NN
#99	Memory clear out

NB. (1) Selected on switch on
(2) Not stored
(3) Selcall tone sequence remains displayed while key depressed.

5.13 FRONT PANEL CONTROLS

a) Type "N" 50Ω RF output connector.
"RF OFF" disconnects the RF output.

b) Modulation input/output socket.

c) External level adjustment.
Provides attenuation for external audio levels of greater than 1V r.m.s.

d) SINAD audio input socket

e) Analogue indication meter.
Provides visual information of SINAD ratio, external modulation level and battery level.

f) Large eight digit LED indication of carrier frequency/modulation rate/data entry and four digit indication of carrier level/modulation level.

g) Display carrier mode.
The LED's indicate carrier frequency/data entry and carrier level.

h) Display modulation mode.
The LED's indicate modulation rate/data entry and modulation level.

i) Data entry keypad.

j) Carrier frequency units select, GHz, MHz or kHz.

k) Carrier level units select, dBm, dBμV, mV and μV pd or emf.

l) Modulation source select.

m) Modulation mode select.

n) Front panel data store and recall.

o) Second function gate key.

p) Cursor position control and up/down digit stepping.

q) Delta key, for use with incremental step mode.

r) Total sweep time entry key.
Also starts/stops the data sweep when in the sweep mode.

s) Local key, enabling front panel control when the instrument is connected to a GPIB controller.

5.14 REAR PANEL CONTROLS

a) Combined mains a.c. input, voltage selector and mains fuse holder.

b) Power on-off switch.

c) Three pin d.c. input socket.

d) d.c. input fuse.

e) 10MHz crystal reference input/output BNC socket.

f) Rear panel RF output option (if fitted).

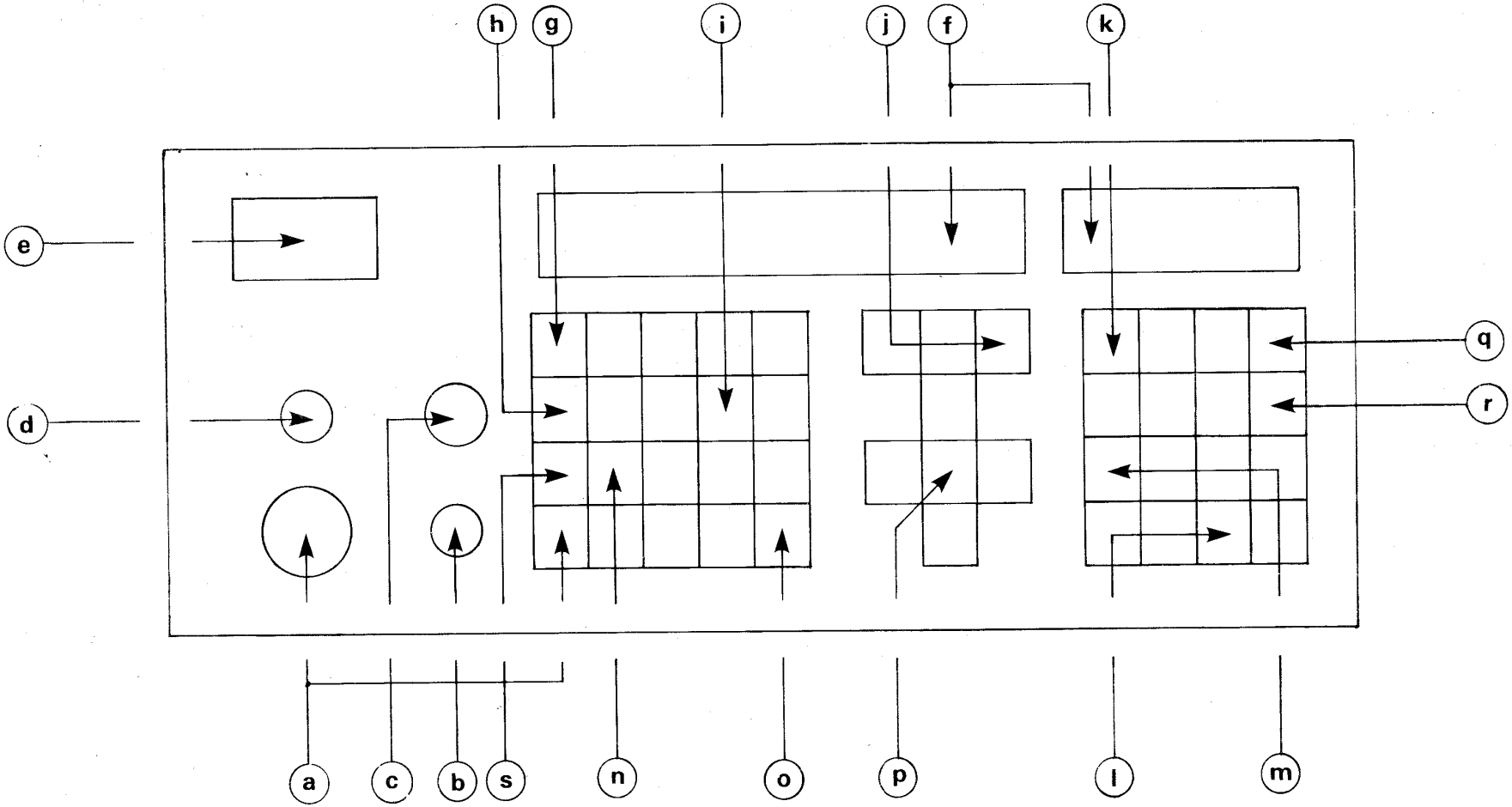
g) Internal 10MHz crystal reference fine adjustment.

h) IEEE 488 socket.

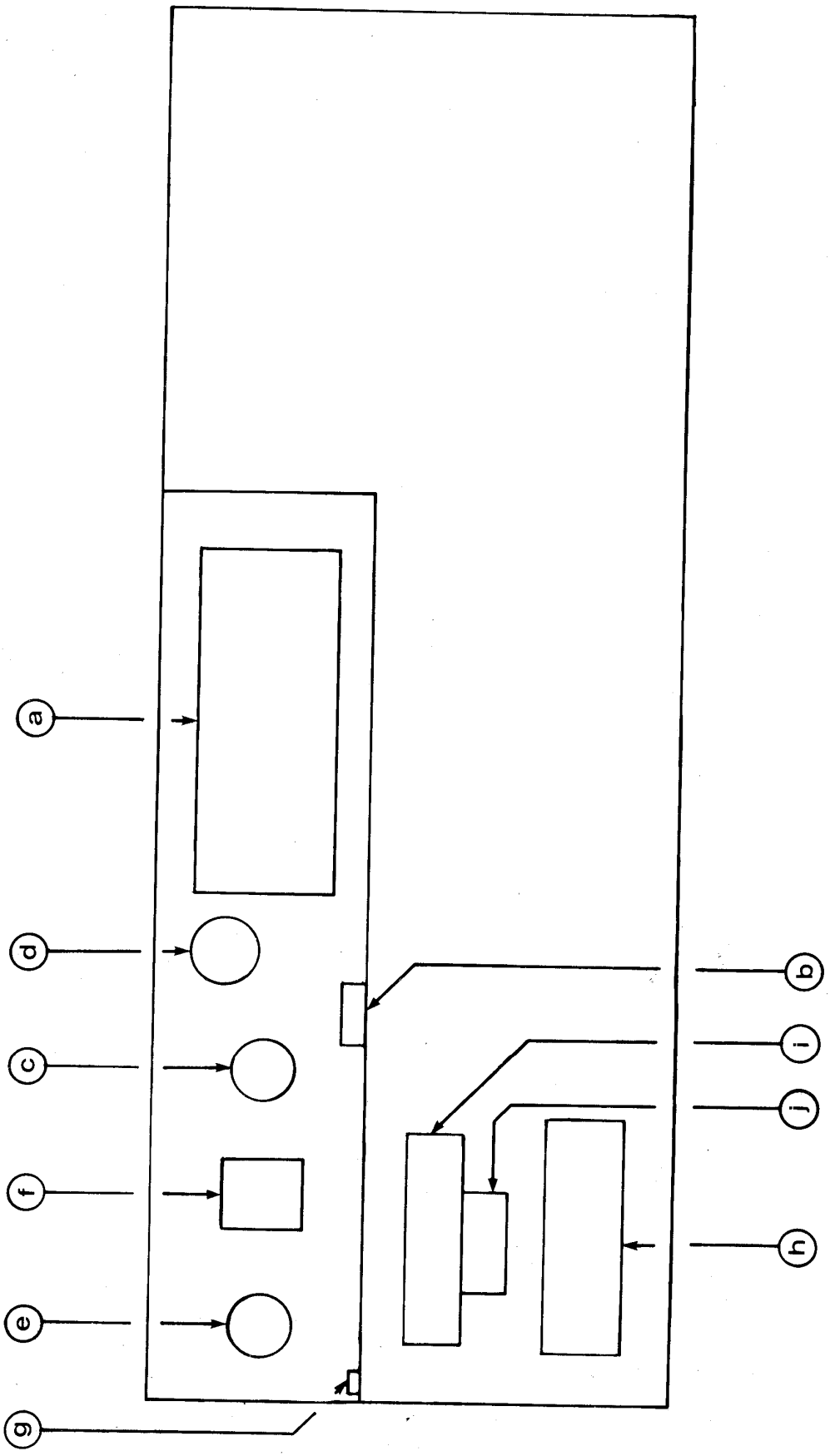
i) HP-IL option socket (if fitted).

j) Auxiliary input socket.

FRONT PANEL CONTROLS



REAR PANEL CONTROLS



5.15 GPIB OPERATION

The software which controls the GPIB interface on the PSG1000 has been written to allow bus control of the instrument to be very similar to the normal front panel control. To control a function using the bus, the same entry sequence is followed as if using the front panel keys. The only difference being that instead of pressing front panel keys in sequence, a series of ASCII strings corresponding to the legends on the keys are sent to the PSG1000 by the bus controller.

e.g. to change the carrier frequency using the front panel keys, the key "DISP CARR" is pressed to switch the display into the carrier mode, followed by the frequency, say 512.000, followed by the units, MHz. To perform this operation on the GPIB the following line would be sent from the controller:

DISPCARR 512.000 MHz

The commands MUST be separated by at least one space.

i.e. DISPCARR (SPACE) 512.000 (SPACE) MHz

A carriage return must be sent at the end of a line as a terminator.

Some of the functions on the front panel have a toggle action, i.e. pressed once they switch a function on, pressed a second time they turn the function off. These can be used in a GPIB programme just as if the user were pressing the front panel keys. However, some additional commands are provided which perform the individual 'on' or 'off' action of these functions. These alternatives give the user the opportunity to make his GPIB programme more readable.

Where there is no common ASCII character for the key legend, a suitable replacement has been found. The corresponding key legend or function is described in the list below in parentheses.

The instrument's bus interface is insensitive to the case of ASCII letters, the commands can be entered using upper and lower case.

Shown below is a list of commands which correspond to the front panel keys.

DISPCARR
DISPMOD
LOCAL
RFOFF
RECALL
STORE
CLEAR

0
1
2
3
4
5
6
7
8
9
.
#

GHz
MHz
kHz

CURSOR
C/ (cursor up)
C\ (cursor down)
C> (cursor right)
C< (cursor left)

dBm
dBμV
%AM

INT1kHz
EXTMOD
kHzFM
μVpd
mVpd
SYNTHRATE
radPM
μVemf
mVemf
DELTA (delta)
SWEEPSECS
DCFM
MODOFF

The following commands perform the single 'on' or 'off' action of a toggle function.

RF-ON
RF-OFF
CSR-ON (cursor on)
CSR-OFF (cursor off)
SYNRT-ON (synthrate on)
SYNRT-OFF (synthrate off)
DCFM-ON
DCFM-OFF
MOD-ON
MOD-OFF

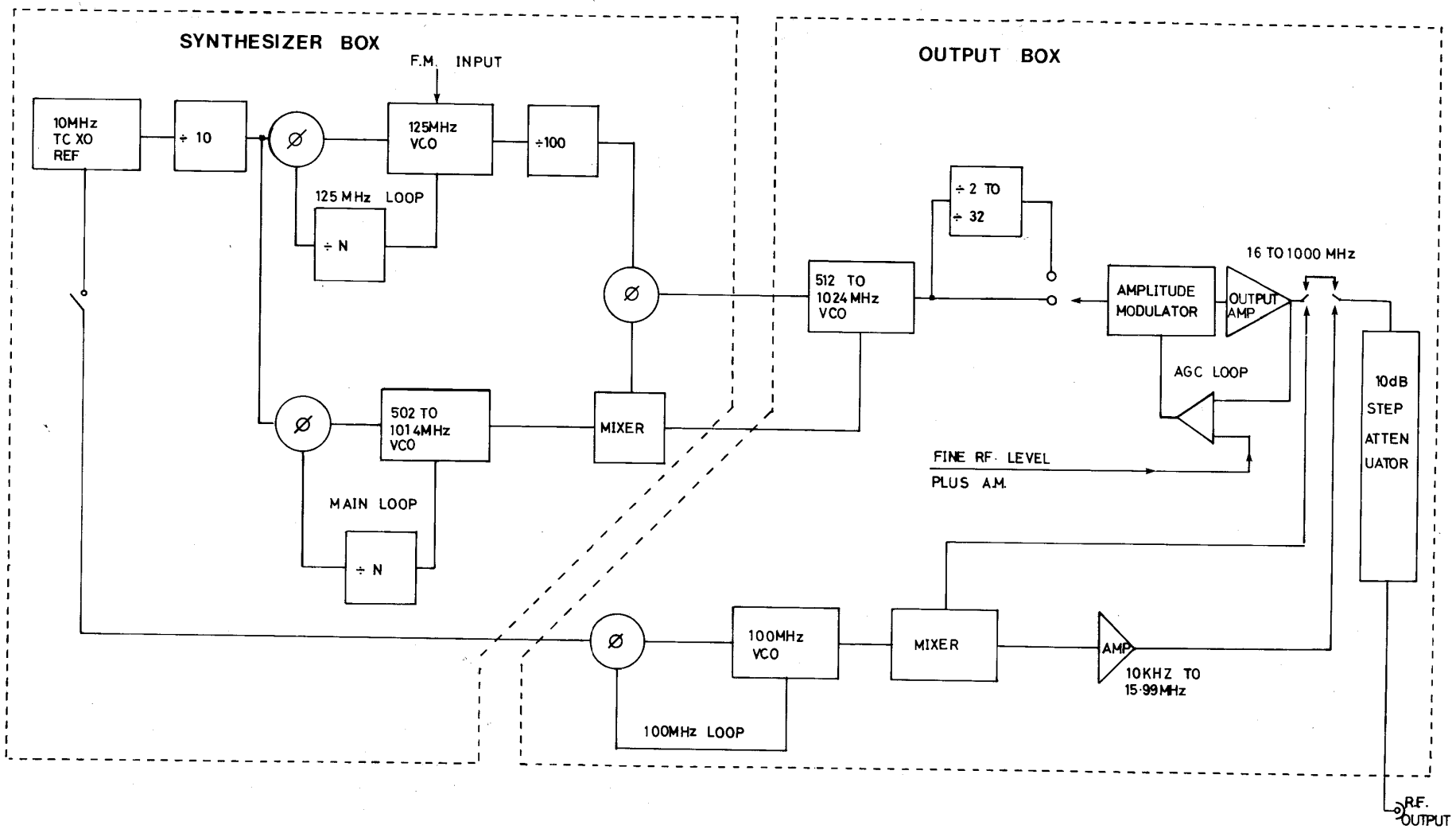
There are some additional commands which perform the same action as some of the gate (#) functions. Separate bus commands have been created for these simply to make the user's programme more readable. These commands are as follows:

INT-REF (same as 0#66)
EXT-REF (same as 1#66)
RELAX-EL (same as #22)

Similarly the command SWEEP performs exactly the same action as SWEEPSECS but will make a programme more readable when initiating a sweep on the GPIB.

6. OVERALL BLOCK DIAGRAM

3ZW10050210 ISS A



7. CIRCUIT DESCRIPTION

7.1 POWER SUPPLY

a) After the power switch SW1, mains power is passed to the primary of transformer TX1, via the voltage selector.

There are three secondary outputs of TX1 to provide low voltage power for the full wave rectifiers D1, BR1 and BR2. D1 is a schottky diode rectifier for maximum efficiency. After smoothing of the rectified signals, linear voltage regulators are utilized to provide stable low noise supplies of +5V, +12V and -10V for the instrument.

Two fixed +5V outputs are provided by U1, U2 and a fixed +12V output by U3.

The -10V regulator, U4, is an adjustable design with P1 setting the output voltage.

The secondary output for the +12V supply is separately rectified by D2, D3 to provide a fast responding advanced warning of power failure for the control circuit board.

b) For operation from an external d.c. supply, a separate inverter secondary winding on the transformer is used.

The coil of relay RL1 is supplied from the d.c. input and operates when the d.c. input is above the minimum level. Diode D12 in series with the relay coil prevents damage due to accidentally reversed d.c. polarity. Relay RL1 isolates the mains input socket and connects the inverter winding to the switching power MOSFETS Q3 and Q4. Drive for Q3 and Q4 is provided by a 70Hz nominal astable multivibrator comprising transistors Q1, Q2 and associated circuitry. This drive level is routed to the control circuit board to provide battery level indication.

7.2 FRONT PANEL AND DISPLAY

a) The front panel membrane switch connections are routed through the display circuit board socket S1 to the control circuit section CT1, via a 20 way ribbon cable.

All LED segments and individual LED indicators on the display circuit board are driven by the serially loaded IC's, U1 to U4. The drivers sink a controlled current for each LED which is set by resistors R1 to R4 and P2.

Resistors R1 to R4 allow the controlled sink current to be varied between each driver U1 to U4 while P2 sets the overall current for all four drivers. This allows adjustment of the brightness of all the LED's.

b) A serial data stream (SB DATA) comprised of 8 bit bursts of data is fed to all four drivers. At each positive going edge of the clock (DP CLOCK) the data steam is accepted. 6 bursts of data are required to load one driver.

When the enable line to any driver is inactive (high) the received data bits are forced to zero and the latched data is unchanged. In the active (low) mode the enable line allows the received data to be accepted. The first burst of data is used for initiallisation while the following 34 bits of data are used to load the driver.

On receipt of the 34th data bit the received data is latched to the driver outputs.

To provide an audible click indication of a front panel key depression relay RL1 is operated by the software for approximately 6ms.

Audio connections for the SINAD input, modulation input/output, external level potentiometer P1 and the front panel meter M1 are routed through the display board on socket S4 to the control board.

7.3 CONTROL

a) Circuit section CT1 forms the heart of the PSG1000, providing the control for the rest of the instrument and containing the GPIB and HPIL interfaces.

The circuit can be considered as 5 distinct sections, these are:

1) The control 'core' comprising the microprocessor, memory, the memory and port decoding and the RESET and RAM protection circuitry.

2) The keyboard interface.

3) The parallel data output to sections CT2 and CT3.

4) The serial data transmission circuit which sends data to the boards in the instrument.

5) The instrument's two digital interfaces, the GPIB and the HPIL.

These sections are described in more detail below.

1) The Microprocessor 'Core'

This comprises and 8085 8-bit microprocessor (U105) running at 2MHz, the obligatory address decoding latch (U104), 48kbytes of ROM (32K in U101, 16K in U102), 8kbytes of battery backed RAM (U103), the address and port decoding (U119 and U120), the RESET circuit (Q101 and half of U109) and the RAM protection latch (U106). As well as providing the system RAM, U103 is also used to store up to 100 front panel settings which are retained when the instrument is switched off. The SOD (serial output data) line on the 8085 is used to drive a peizo sounder and to provide a 'sweep synch out' signal.

2) The Keyboard Interface

The keyboard interface comprises an 8155 peripheral interface IC (U124) and

an 8 input OR gate (U125). Six lines of port A on 8155 form the 'send' lines of the keyboard matrix and the 8 lines of port B are the keyboard 'return' lines. In its normal state all the send lines are held high and all the return lines are OR'ed by U125 to generate an interrupt when a key is pressed. In response the microprocessor initiates a keyboard scan, taking each send line high separately and monitoring the return lines to see which key has been pressed.

Port C is used to read the output of U127, an interrupt priority encoder. This allows several peripheral devices to use a common interrupt line to the microprocessor. The 8155 IC also contains a programmable timer which is used in the implementation of the instrument's sweep function.

3) The Parallel data Transmitter

Data is sent to the circuit sections CT2 and CT3 via 6 latches (U110 to U115). This data bus to these devices is buffered to from the main system by U121. Since this device is only selected when data is sent to one of the 6 latches the amount of bus generated 'noise' on the board is reduced.

4) The Serial Data Transmitter

Circuit sections CT2 and CT3 are located on the same circuit board as section CT1 so the 8 bit parallel data bus described in 3) is the most direct transfer. In contrast, in order to reduce the amount of wiring between boards and to restrict the level of noise generated by the microprocessor busses, a serial system is used to transfer data to other boards in the instrument.

The serial data transmitter comprises U117, U116, U122, U123, U108 and half of U107. The microprocessor initiates a serial transmission by writing a data byte to latch U116. This action also starts counter U123 which is used to sequentially select all the 8 inputs to data selecter U122. The resulting serial data on the output of U122 is sent with the serial clock (also derived from counter U123) to the other circuit boards.

The microprocessor then writes a byte to latch U117 which provides the enable signals for the serial receive latches on the other circuit boards.

The serial clock to the range divider board and the synthesizer board is buffered and gated by U108-C and U108-D. This enables this signal to be 'switched off' when the serial data is destined for another board. The gateing signal is provided by a port line from the 8155. The serial data rate is 1 bit/8µs.

A second serial data line to the range divider board doubles up as an interrupt input when the serial data circuit is not in operation. This interrupt warns the microprocessor of a 'reverse power' condition on the instrument's RF output.

5) The GPIB and the HP-IL interfaces

The GPIB and the HP-IL interfaces are implemented using proprietry IC's which interface directly to the microprocessor. The GPIB comprises U128, U129 and U130. U128 is an intelligent GPIB interface IC and performs all the necessary bus protocol when transferring data on the bus. U129 and U130 are receiver/driver IC's for the bus data and control lines respectively. The HP-IL comprises U131, U132 and T101 (a HP-IL pulse transformer). Like U128, U131 is an intelligent interface IC. The interrupt outputs from the two interfaces go to the interrupt priority encoder U127.

The Software

The microprocessor spends most of its time in a 'sleep' mode and only wakes up when it is interrupted by the keyboard, the programmable timer, GPIB or the HP-IL interface or a 'reverse power' condition on the RF output. On receiving an interrupt the microprocessor scans these sources to determine which one sent the interrupt. It then takes the appropriate action and returns to its 'sleep' mode.

The exception to this is when the instrument is being controlled by the GPIB or the HP-IL. In these cases, when an interrupt is first identified as

coming from one of these two sources, the programme jumps to a secondary loop which continually searches for characters from the appropriate interface and executes valid commands. The programme returns to the main loop either by a direct command from the interface or by the user pressing the LOCAL key on the front panel (the only key which is recognised is this mode).

b) Synthesized audio signals in the range 10Hz to 9.999kHz are generated by section CT2. Ic's U201 to U204 form a 4 decade BCD rate multiplier, clocked at 2MHz. The resulting series of pulses is divided by 4 with U207 to produce a square wave output. Further division by 5, U208 and 10, U209 gives a maximum 10kHz square wave input to the switched capacitor filter, U210. The filter is clocked at a rate of 50 times the input frequency by the signal from pin 13 of U207.

For audio frequencies of < 1kHz an extra divide by 10, U205, is switched in by the gate U206.

The sine wave output from pin 3 of U210 is passed through an active low pass filter to remove unwanted signals at the clock frequency. This filter has 3 ranges, < 100Hz, < 1kHz and < 10kHz, with the filter capacitors switched in by gates U211-C, U211-D. The audio output at pin 2 of U210 is adjusted in level by P201 and passed to the modulation control section, CT3.

For 2 tone modulation applications when the audio synthesizer is mixed with another source, the synthesizer level is reduced to approximately 20% of the normal level when gate U212-A is enabled.

c) Control of the modulation level is performed by section CT3.

The 2MHz clock from CT1 is divided by 2 with U308, then successively by 10 with U309 to U311. The resulting 1kHz fixed square wave is passed to the input of the switched capacitor filter, U312.

This filter is clocked at 100kHz by the signal from pin 12 of U309 and the resulting 1kHz sine wave passed to the modulation control section via gate U301-C. This gate is disabled for EXT MOD and the external signal passed through gate U301-B to amplifier U302-A. Summing of the synthesizer and 1kHz signals is performed by R302, R304 and passed to the modulation level DAC via amplifier U302-B.

U315 comprises a 10 bit DAC enabling the audio level at pin 1 of U305-A to be adjusted in 0.1% steps by the 10 bit modulation level code from CT1.

When INT 1kHz is selected a fixed level of 1V r.m.s. is routed to the front panel modulation socket via gate U303-A and amplifier U316. Enabling the synthesizer routes the adjustable modulation signal through gate U303-B to the modulation socket. This provides an audio synthesized output adjustable both in frequency and level.

For FM and phase modulation the audio signal is routed to the FM drive amplifier U307-A.

A stable reference voltage for the RF level control is generated by zener diode D301 and attenuated by P303.

When AM is selected the modulation signal is summed with the RF level control voltage in amplifier U305-B and the combined signal passed to the RF level control DAC, U306. This combined signal is attenuated in fixed steps corresponding to 0.1dB steps of the RF level. These steps are controlled by the 10 bit AGC control code from CT1.

Amplifier U307-B provides the combined RF level control and AM drive signal for the output amplifier.

d) Section CT4 comprises the SINAD and front panel meter drive circuits.

The 1kHz SINAD input signal is fed to the AGC amplifier U401 whose output remains constant at approximately 200mV pk-pk over an input level variation of more than 40dB. U402 comprises a switched capacitor 1kHz notch filter

clocked at 100kHz. The resulting noise and distortion signal is amplified by U407 and gated through U405-B to the meter drive circuit.

When enabled, the battery level and external modulation signals are also routed through U405 to the meter drive.

The audio signal is detected by U404 and U406 which has a true r.m.s. response. The d.c. output at pin 14 of U404 is then further amplified by U403-B to drive the front panel meter.

7.4 SYNTHESIZER

a) The main reference for the synthesizer is located in section HS1. Power connections are +5V at pin X102 and +12V at pin X101. XTL1 is a temperature compensated 10MHz crystal which is coarse tuned by P101 and fine tuned by the back panel potentiometer. The instrument may be referenced from XTL1 or externally from a 10MHz source connected to the back panel input.

When internal reference is selected (0#66), pin 11 of U202 (external select line) is set high. The 10MHz signal is passed through U102-C, U102-D and pin 3 of U102-A is set high. This gates the 10MHz signal to the input of U101 and to RL1. U101 divides the clock by 10 to provide a 1MHz signal for the synthesizer.

When the down converter range is selected (< 16MHz) RL1 is enabled by pin 11 of U603, routing the 10MHz reference to the output box.

For external reference (1#66) the microprocessor sets pin 11 of U202 low, forcing pins 8 and 11 of U102 high and reverse biasing D102. The back panel input via D101 is level converted by Q101 and inverted by U102-A.

b) The FM oscillator is located in section HS3. Power connections are +12V at X302 and -10V at X303. FET Q301 and varactor diodes D301 and D302 form a voltage tuned oscillator. The tuning voltage at X301-2 is composed of a d.c. voltage and the FM drive signal.

The FM drive signal is adjusted to compensate for the reduction of FM deviation when the main UHF output oscillator is divided down to form other RF ranges.

c) Section HS2 contains the FM step loop. Power connections are +5V at S201-5, +12V at S201-3 and -10V at S201-4. The FM loop phase locks the FM oscillator over the range 125.0MHz to 126.25MHz. For carrier frequencies of <128MHz the FM loop is locked in 1kHz steps to produce an output frequency resolution of 10Hz. Above 128MHz the step loop goes in 1.25kHz steps for an output resolution of 100Hz.

Serial latch U202 loads the synthesizer IC U203 with 8 bit data, controlled by the enable line EN0. A common enable signal (S201-8) is used for the FM step loop and the UHF step loop. A low level on pin 4 of U211 gates the enable via U214-A, U213-A, U213-B to the FM step loop latches. A high level on pin 4 of U211 gates the enable line to the UHF step loop latches (U603, U604). Refer to the latched data information on the next page.

The synthesizer integrated circuit, U203, contains 3 programmable counters "R, "N" and "A" which are set by 8 internal latches. These latches can be independently programmed by address lines DS0, DS1 AND DS2. The latched data is transferred to the counter coincident with data transfer to latch 1 (address 000). This is the final latch addressed during a frequency change.

LATCHED DATA FOR FM LOOP

SYNTHESIZER (+R, +N, +A LATCHES)

PIN No										
4	Q1	D0	-	N2	N6	A0	A4	R0	R4	R8
5	Q2	D1	-	N3	N7	A1	A5	R1	R5	R9
6	Q3	D2	N0	N4	N8	A2	A6	R2	R6	R10
7	Q4	D3	N1	N5	N9	A3	-	R3	R7	-
14	Q5	DS0	0	1	0	1	0	1	0	1
13	Q6	DS1	0	0	1	1	0	0	1	1
12	Q7	DS2	0	0	0	0	1	1	1	1
11	Q8	$\overline{\text{EXTERNAL REFERENCE SELECT}}$								

LATCHED DATA FOR UHF LOOP

SYNTHESIZER (+R, +N, +A LATCHES)

PIN No										
4	Q1	D0	-	N2	N6	A0	A4	R0	R4	R5
5	Q2	D1	-	N3	N7	A1	A5	R1	R5	R9
6	Q3	D2	N0	N4	N8	A2	A6	R2	R6	R10
7	Q4	D3	N1	N5	N9	A3	-	R3	R7	-
14	Q5	DS0	0	1	0	1	0	1	0	1
13	Q6	DS1	0	0	1	1	0	0	1	1
12	Q7	DS2	0	0	0	0	1	1	1	1
11	Q8	DOWN CONVERTER REFERENCE ENABLE								

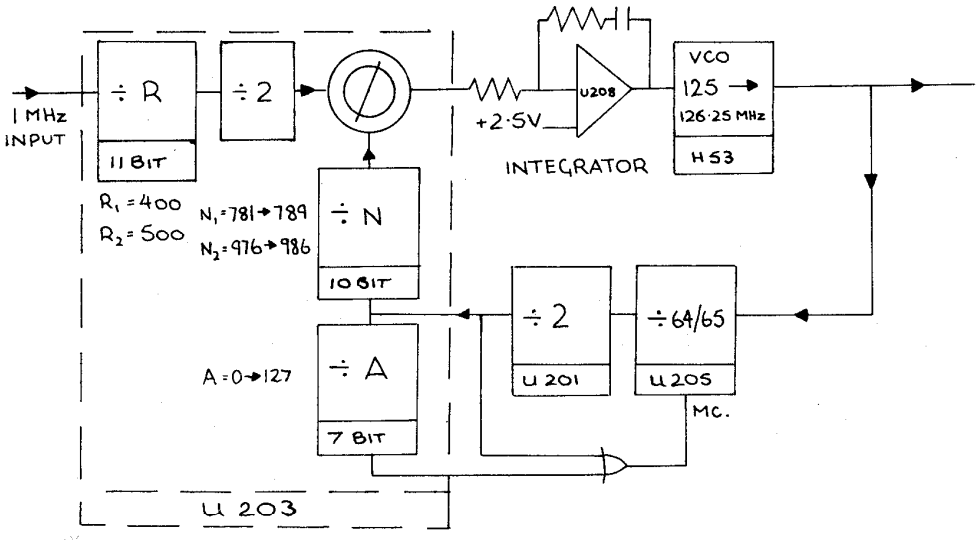
MODULATION RANGE CONTROL &

SWITCHING LATCH

PIN NO						
4	Q1	SYNTHESIZER DATA STEERING	H-UHF STEP LOOP L-FM STEP LOOP			
5	Q2	$\overline{\text{DC FM SELECT}}$				
6	Q3	FM OFF SELECT				
7	Q4	10kHz SELECT				
		FM RANGE	+1	+2	+4	+8
14	Q5	D0	L	L	L	L
13	Q6	D1	L	L	L	H
12	Q7	D2	L	L	H	H
11	Q8	D3	L	H	H	H

FM MODULATION DAC SETTING

	FM RANGE	<10kHz			>10kHz					
FREQUENCY RANGE MHz	MAXIMUM DEVIATION KHz	2.49	4.99	9.99	2.5 - 25	5.0 - 50	100	200	400	800
.010 - 15.999 99		+1	+1	+1	-	-	+1	NA	NA	NA
16 - 31.999 99		+1	NA	NA	+1	NA	NA	NA	NA	NA
32 - 63.999 99		+1	+1	NA	-	+1	NA	NA	NA	NA
64 - 127.99 99		+1	+1	+1	-	-	+1	NA	NA	NA
128 - 255.999 9		+2	+2	+2	-	-	+2	+1	NA	NA
256 - 511.999 9		+4	+4	+4	-	-	+4	+2	+1	NA
512 - 1000		+8	+8	+8	-	-	+8	+4	+2	+1



The "R" counter is set either to 500 or 400 to give phase detector reference of 1kHz or 1.25kHz. In the locked condition "N" and "A" counters are programmed so that the VCO frequency is divided down to either 1kHz or 1.25kHz exactly. The divider chain is composed of U205 (÷64/65) and U201 (÷2). A modulus control output derived from the "A" counter sets the combined divide to ÷ 128 (A=0) or ÷ 129 (A $\geqslant$ 1).

In the unlocked condition the phase detector outputs (pins 1, 2 U203) force the integrator (U208-A) output in the required direction for the FM oscillator to lock.

The FM drive enters the synthesizer box on S201-9 from the control board. This level varies with the set modulation deviation, 1V r.m.s. corresponding to 100kHz deviation.

For FM deviation of < 10kHz a switched attenuator is selected by pins 7 of U211 and U215C, with P203 calibrating this range.

The modulation signal is then buffered by amplifier U210-A and passed to the FM range DAC, U212. Depending upon the carrier frequency range, the DAC divides the modulation signal by 1, 2, 4, or 8 (refer to latched data information for settings). This control information is strobed into U211 by the enable line EN1 from the microprocessor. When FM is not selected the modulation signal is shorted to ground by U215-D.

Amplifier U209-B provides gain control for the modulation with P201 the calibration adjustment. The FM drive signal is then combined with the integrated output in the difference amplifier U209-A, thus providing tuning and modulation for the FM oscillator. For high modulation rates a boost circuit comprising C225 and R230 is used.

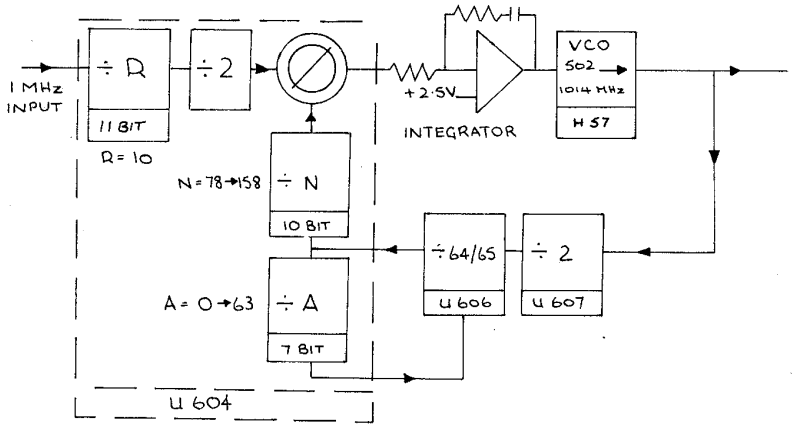
At low rate modulation deviations the normal closed loop synthesizer action would remove this deviation.

When DC FM is selected (pin 5 of U211) the FM step synthesizer is disabled, with the digital and analogue outputs from the phase detector switched to open circuit, U207-A and U207-B.

d) The main UHF step oscillator is located in section HS7. Power connections are +12V at X605 and -10V at X606. Transistor Q701 and varactor diodes D701, D702 form a voltage tuned oscillator covering the frequency range 502MHz to 1014MHz. The UHF step loop phase locks this oscillator to the crystal reference in steps of 100kHz or greater.

e) Section HS6 contains the UHF step loop. Power connections are +5V at X604, +12V X602 and -10V at X603. Serial data present at pin 2 of U603 is clocked into the 8 stage shift register, U603. Transfer of data is controlled by the enable line EN0.

A high on pin 4 of U211 gates the enable EN0 as active data is transferred simultaneously into the output latches of U603 and the synthesizer latches U604.



The "R" counter is set to 10, to give a reference of 50kHz at the phase detector. In the locked condition "N" and "A" counters are programmed such that the VCO output is divided down to 50kHz exactly.

The divider chain is comprised of U607 (÷ 2), U606 (÷ 64/65) and U604 (÷ N).

A modulus control signal derived from the "A" counter switches U606 to either ÷ 64 (A=0) or ÷ 65 (A $\geqslant$ 1).

In the unlocked condition the phase detector outputs (pins 1, 2 of U604) force the integrator (U605) output in the direction required for the UHF step oscillator to lock. This oscillator is locked exactly 10MHz below the output UHF for steps > 100kHz.

f) The UHF sum loop is located in section HS5. Power connections are +5V at X504 and +12V at X503. The UHF step oscillator is buffered by amplifiers U608, U505 and passed to the local oscillator input of mixer U503. Amplifier U504 buffers the UHF output oscillator signal which is fed to the RF input of mixer U503. In the locked condition the mixer IF output is 10MHz. This signal is passed through a low pass filter comprising C507-C509, C503, C504 and amplified by U502.

The 10MHz signal is then divided by 8 (U501) to give a 1.25MHz signal which forms one input of the sum phase detector, U509. A 1.25MHz reference signal for this detector is obtained by dividing the output of the FM step loop by 100 with U206.

g) Section HS4 contains the sum integrator. Power connections are +12V at X403 and -10V at X404. The 2 outputs from the sum phase detector, U509, are passed to the sum integrator, U401, whose d.c. output voltage tunes the output UHF oscillator. In the unlocked condition the integrator tunes the output UHF oscillator until a frequency is reached where the IF output of mixer U503 is exactly 10MHz.

If the tuning voltage of the output and step loop UHF oscillator is vastly different the IF output from U502 will fall outside the maximum operating frequency of the ÷ 8 counter U501. To prevent this occurrence a lock aquisition circuit comprising U601, U602, D605, D606 and D607 is utilised which compares the tuning voltage of the 2 UHF oscillators.

If the output UHF oscillator tuning voltage exceeds the step oscillator voltage by more than +1.2V then pin 7 of U602 goes low and is inverted by U601-A. This forces the sum integrator low via D401, reducing the output UHF oscillator tuning voltage (and frequency).

Conversely, if the tuning error is more than -1.2V, pin 1 of U602 goes low and is inverted by U601-D. This forces the sum integrator high via D402, increasing the output UHF oscillator frequency. The correction signal on U601-D is latched so the integrator output will be forced up through the operating window until the latch is reset by the tuning error exceeding +1.2V.

This ensures the 2 UHF oscillators are phase locked 10MHz apart and track together over wide variations of their respective tuning voltages.

7.5 Range Divider

a) An octave tuned varactor oscillator (section RD2) comprising transistor Q201 and varactor diodes, D201, D202, provides a stable RF output covering 512MHz to 1024MHz. This oscillator is phased locked to the synthesizer UHF oscillator via the tuning line.

Amplifier U1 provides a buffered oscillator signal for the UHF synthesizer while amplifier U2 isolates the oscillator from the digital dividers. These divider stages, covering ÷2 to ÷32, are switched in for each RF range. The serial latch U5 controls the range selection. By using digital dividers only one UHF oscillator is required to cover the range 16MHz to 1000MHz.

Each digital divider output is followed by a voltage tuned low pass tracking filter to produce a sine wave output from the square wave input. The tuning voltage for the varactor tuned filters is derived from the UHF oscillator tuning voltage and buffered by amplifier U3.

All the digital divider outputs have individual PIN diode isolating switched, routed through to a common amplifier U12.

The resulting 16MHz to 1000MHz signal is passed through to the output amplifier at pin X3.

b) Output frequencies in the range 10kHz to 15.99MHz are derived by mixing a fixed 100MHz source with 100.01MHz to 115.99MHz from the divider ranges. This down converter range is located in section RD3 of the range divider.

The 100.01MHz to 115.99MHz RF input signal is routed to the mixer U300 from the output attenuator. The down converter section is switched in when required by transistors Q300 and Q301 in the +12V and +5V power rails. FET Q303 and inductor L300 form the 100MHz voltage tuned local oscillator which is phased locked to the main 10MHz crystal reference. The 100MHz signal is divided by ten with U301 and passed to the phase detector U302 which is referenced from the internal 10MHz crystal in the synthesizer. Feedback amplifier U303 completes the loop and locks the oscillator to exactly 100MHz.

The IF output from the mixer is passed through a 20MHz low pass filter comprising L303, L304, L305 and amplified by Q307.

The 10kHz to 15.99MHz signal is then passed to the output attenuator at pin X8.

c) The down converter RF switching, 10dB fixed attenuator steps and the reverse power protection relay are operated by the output control section RD4. Serial latch U400 selects which relay to operate.

All the switching for the relay coils is designed for minimum power consumption. For example, the down converter select has a series resistor R402 which is shorted out by transister Q401 for approximately 5ms after Q400 is turned on. This peak voltage of approximately +4.0V at pin X10 ensures the relay switches correctly.

After this 5ms period transistor Q410 is turned off and the coil voltage reduces to a holding level of about +1.5V.

To protect the RF attenuator from reverse power damage a series relay is provided to isolate the attenuator. The detector diodes are located in the output attenuator and the detected level at points X21, X22 is passed to amplifier U402-A.

When the preset trip level is exceeded the output of U403-B goes high, triggering the reverse power latch U401 and operating the protection relay.

To prevent the reverse power detector self tripping on the instruments own high level output of +13dBm, the trip level is set at +6.0V. For additional protection at lower RF levels ($\leqslant$ -3dBm) this trip level is reduced to +1.2V when gate U402-D is enabled.

7.6 Output Amplifier

a) The combined RF signal from pin X3 of the range divider is boosted to the maximum level of +13dBm by the output amplifier which also contains the 10dB step attenuator.

For carrier frequencies of < 64MHz relay RL8 is energised switching in the low pass filter comprising L4, L5, C38 and C39, thus reducing unwanted higher frequency harmonics.

An adjustable RF attenuator composed of PIN diodes D1, D2 and D3 forms the amplitude modulator and AGC level control. Amplifier U2 boosts the signal to a maximum of +13dBm output. To control the RF level in 0.1dB and 1dB steps a feedback AGC loop is utilised. The RF level is detected by schottky diode D7 and filtered by R18 and L2. Transistors Q1 and Q2 form a constant current source to provide a small forward bias current for D7 thus extending its dynamic range.

The AGC loop is completed by the error amplifier U1 whose output controls the PIN diode attenuator bias through R4. This AGC loop also acts dynamically to control the amplitude modulation depth. The combined d.c. level control voltage and amplitude modulation signal is applied to pin 2 of amplifier U1.

The RF signal is then passed through R20 to the 10dB step attenuator.

b) For carrier frequencies of < 16MHz relay RL1 routes the RF signal to the down converter section and allows the IF signal to the attenuator through the low pass filter comprising L3, C34 and C35.

The output attenuator is arranged in sections of 10dB, 20dB, 30dB and 60dB (30dB + 30dB) switched in by relays RL2 to RL6.

Carrier levels in the range + 13dBm to -2.9dBm are controlled by the fine level AGC loop with no 10dB attenuator switched in. At a carrier level of -3.0dBm the AGC loop sets the output amplifier level to +7dBm and a 10dB

attenuator is switched in. This combination allows the RF level to be adjusted in a 0.1dBm steps over the entire carrier level range.

To protect the attenuator and output amplifier from excessive reverse voltages a protection relay, RL7, is incorporated. Diodes D8 to D11 detect the RF signal in the attenuator. When an excessive signal is detected relay RL7 disconnects the attenuator from the instruments RF output connector.

When the instrument is switched off relay RL7 is normally in the open circuit mode thus providing additional protection.

7.7 Pulse Modulator

a) When this option is fitted it is located in series with the main RF output between the output box and the front panel connector.

Relays RL1 and RL2 short out the pulse modulator when not required thus minimising RF level accuracy errors.

To enable the pulse modulator the pulse mod enable line is connected to +5V.

PIN diodes D3, D4, D5 and D6 form a compound series switch with high isolation and low insertion loss. In the carrier on mode, transistor Q1 is turned off allowing diodes D4 and D5 to be forward biased through R3 and R4. Simultaneously diodes D3 and D6 are reverse biased thus providing a low impedance path from RF input to RF output.

When the pulse input line is grounded (carrier off), transistor Q1 is turned on reverse biasing D4, D5 and forward biasing D3 and D6. This results in maximum attenuation between the RF input and RF output.

8. CALIBRATION PROCEDURE

8.1 AUDIO

All adjustments are located on the control C/B

a) Select INT 1kHz and monitor the audio modulation output on a true r.m.s. voltmeter., Adjust P306 (1kHz LEVEL) for a reading of 1.00V r.m.s.

Select 0.00% AM and monitor pin 1 of U305 with a DVM. Adjust P301 (DAC OFFSET) for a reading of 0.00mV.

Monitor pin 7 of U307 with the DVM. Select RF OFF and adjust P304 (DAC OFFSET) for a reading of -10.0mV $\pm$ 0.5mV.

Select SYNTH RATE at 1.00kHz and 99.9% AM. Adjust P201 (SYNTH LEVEL) for an audio modulation level reading of 1.00V r.m.s.

b) Select EXT MOD and feed in a 1.00V r.m.s. 1kHz sine wave to the modulation input BNC. Set the front panel modulation level control full clockwise.

Monitor pin 14 of U404 with the DVM. Adjust P405 (DETECTOR CAL) for a reading of 1.10V $\pm$ 0.05V. Remove the external signal and adjust P406 (DETECTOR OFFSET) for 0.00V at pin 7 of U403.

Re-connect the external signal and adjust P407 (METER CAL) for FSD on the front panel meter.

c) Connect the INT 1kHz audio modulation signal to the SINAD input.

Adjust P402 (NOTCH ADJ) for minimum 1kHz signal at test point X401, typically 40mV pk-pk.

Remove the SINAD input and adjust P404 (SINAD OFFSET) for 0.00mV at pin 6 of U407.

Feed in a standard 25% distorted 1kHz signal to the SINAD input.

Adjust P403 (SINAD CAL) for a front panel meter reading of 12dB. Re-check P404 adjustment as above.

d) Connect a +12V d.c. source (+24V for option) to the power supply and monitor the source voltage with a DVM.

With +12.0V input, adjust P401 (BATTERY CAL) so the front panel battery level indiaction is on the red/black marker.

8.2 SYNTHESIZER

a) Select 1GHz and monitor the RF output on a frequency counter referenced from a frequency standard.

Adjust P101 (FREQ TUNE HS1) for a reading of 1GHz $\pm$ 100Hz.

Fine tune the frequency using the back panel control.

b) Monitor the FM loop tuning voltage on socket X301 with a DVM.

Select 512.0MHz and adjust the core of L301 for reading of -1.0V $\pm$0.2V on the DVM.

8.3 SPECTRAL PURITY

a) Select 512MHz and monitor the RF output on a spectrum analyser, scan width 1MHz per division.

Adjust P401 (OFFSET ADJUST) located in section HS4 on the synthesizer C/B for minimum amplitude of the 1.25MHz reference sidebands, typically -65dBc.

b) Select 256MHz and +7dBm. Monitor pin 3 of U4 on the range divider with a DVM.

Adjust P2 (FILTER TUNE) for a reading of 1.0V ±0.1V.

Check the harmonic content is < -25dBc.

8.4 RF LEVEL CALIBRATION

a) Select 100MHz and +13.0dBm. Monitor the RF output on a power meter. Adjust P303 (RF LEVEL CAL) on the control C/B for a reading of +13.0dBm.

Select -2.0dBm and adjust P2 (DETECTOR BIAS) on the output amplifier C/B for a reading of -2.0dBm. Re-check the +13.0dBm setting.

b) Select 10.0MHz and +13.0dBm. Adjust P300 (IF LEVEL) on the range divider C/B for a reading of +13.0dBm.

8.5 AM CALIBRATION

a) Allow the unit to warm up for 30 minutes before making adjustments.

Select 100MHz, +6.9dBm and 80% AM INT 1kHz. Monitor the RF output on a modulation analyser.

Adjust P302 (AM CAL) on the control C/B for a reading of 80.0%.

b) Select -2.9dBm and adjust P1 (AF SHAPER) on the output amplifier C/B for minimum modulation distortion, typically 1%.

Check the difference between 80% AM at +6.9dBm and -2.9dBm is less than 1.0% AM. If not, slightly re-adjust P2 (DETECTOR BIAS) and re-check the RF level calibration.

8.6 FM CALIBRATION

a) Select INT 1kHz, 99.9kHz FM and monitor pin 1 of U307 (on the control C/B) with a true r.m.s. voltmeter.

Adjust P305 (FM CAL) for a reading of 1.00V r.m.s.

Monitor pin 1 of U209 on the synthesizer C/B with a DVM. Select MOD OFF and note the d.c. offset.

Deselect MOD OFF and adjust P202 (OFFSET ADJUST HS2) for the same d.c. offset as above.

b) Select 100MHz, 0dBm, INT 1kHz, 99.9kHz deviation.

Monitor the RF output on a modulation analyser. Adjust P201 (FM CAL, HS2) for a reading of 99.9kHz.

Change the deviation setting to 5.0kHz and adjust P203 (10kHz ADJUST HS2) for a modulation analyser reading of 5.0kHz.

9. MAINTENANCE

9.1 GUARANTEE

The equipment supplied by Farnell Instruments Ltd. is guaranteed against defective material and faulty manufacture for a period of twelve months from the date of despatch. In the case of material or components employed in the equipment but not manufactured by us we allow the customer the period of any guarantee extended to us.

The equipment has been carefully inspected and submitted to comprehensive tests at the factory prior to despatch. If, within the guarantee period, any defect is discovered in the equipment in respect of material or workmanship and reasonably within our control, we undertake to make good the defect at our own expense subject to our standard conditions of sale. In exceptional circumstances and at the discretion of the Service Manager, a charge for labour and carriage costs incurred may be made.

Our responsibility is in all cases limited to the cost of making good the defect in the equipment itself. The guarantee does not extend to third parties, nor does it apply to defects caused by abnormal conditions of working, accident, misuse, neglect or wear and tear.

9.2 MAINTENANCE

In the event of difficulty or apparent circuit malfunction, it is advisable to telephone (or telex) the Service Department or your local Sales Engineer or Agent (if overseas) for advice before attempting repairs.

For repairs and recalibration it is recommended that the complete instrument be returned to:

The Service Department,
Farnell Instruments Limited.,
Osborn House,
Sandbeck Way,
Wetherby, West Yorks. LS22 4DH

Tel. 0937 61961 Telex. 557294 Fax. 0937 66908

When returning the instrument please ensure adequate care is taken with packing and arrange insurance cover against transit damage or loss. If possible re-use the original packing box, following the instructions below:

Wrap the instrument in anti static polythene and tape up then place into primary box ensuring the feet are next to the polystyrene supports. Wrap up accessories and instuction/service manual and place into the primary box in the space left between the polystyrene supports. Seal the primary box, fit the corner blocks and place into the outer box ensuring the corner blocks are positioned correctly. Finally, seal the outer box.

9.3 ADJUSTMENTS

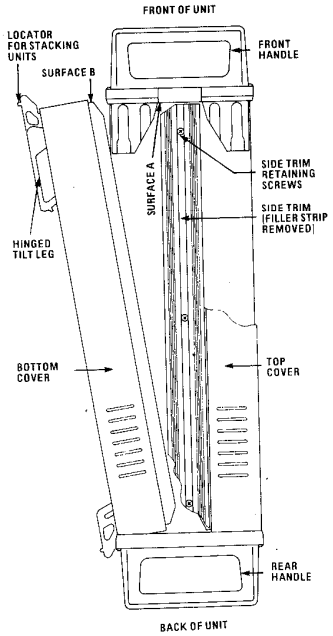


FIG 1

TO REMOVE COVERS (FIG 1)

1. Prise out plastic filler strips from the side trims.

2. Remove side trim retaining screws (4 screws) Remove side trims.

3. Working from front: for each cover, slide backwards to clear recess in front handles. Widen the front to clear the front handles. Hinge cover away from the unit to just clear front handles. Then pull forwards.

10. L O C A T I O N D I A G R A M S

10.1 CONTROL TRAY ASSEMBLY CTM

a) The control circuit board (CT) is housed in the control tray assembly and is divided into 4 sections listed below:

Microprocessor control, CT1
Audio synthesizer, CT2
Modulation control, CT3
SINAD and meter drive, CT4.

10.2 SYNTHESIZER BOX ASSEMBLY SB

a) The synthesizer circuit board (HS) is housed in a fully screened RF enclosure and is divided into 7 sections listed below:

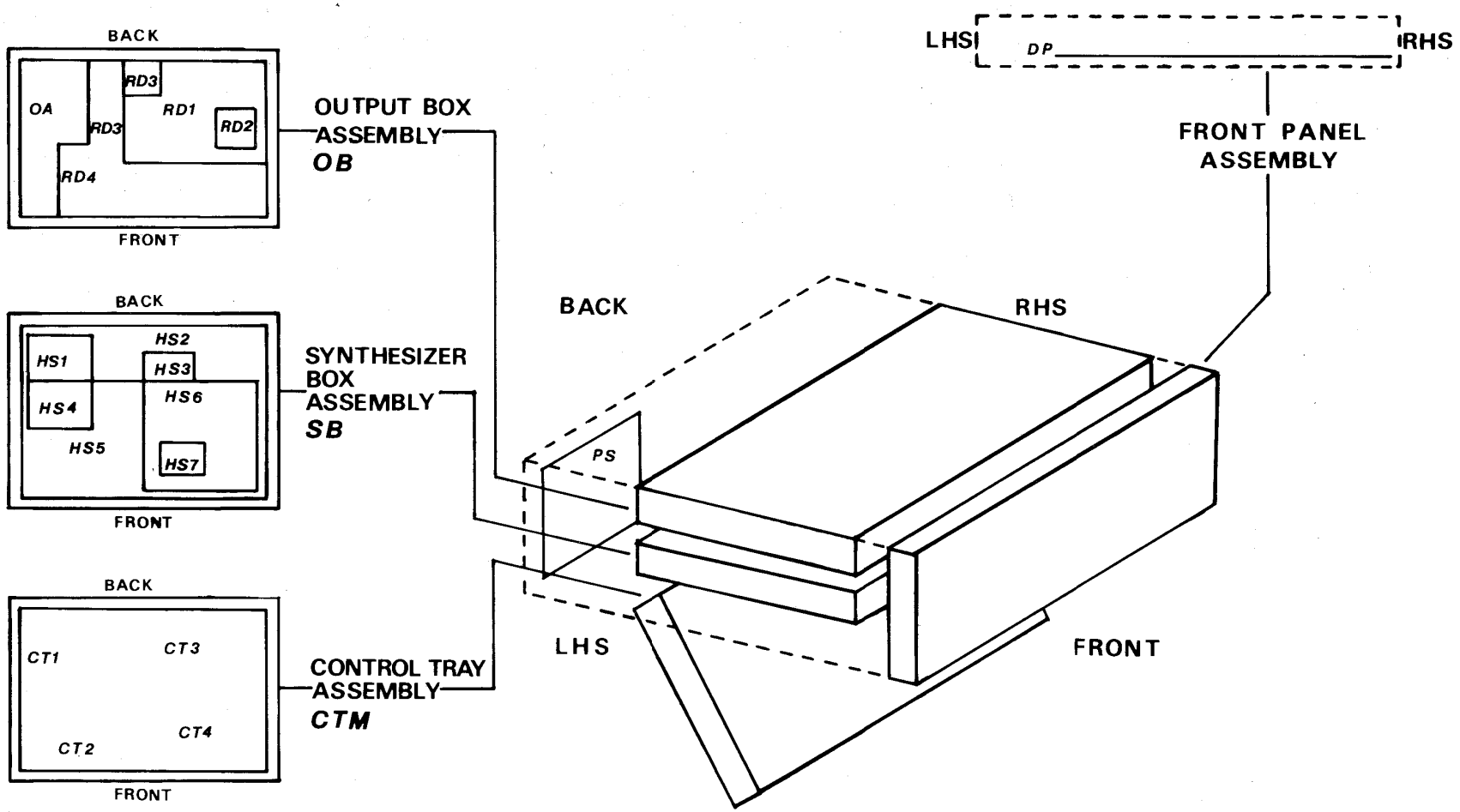
10MHz reference oscillator, HS1
FM step, HS2
FM oscillator, HS3
Sum integrator, HS4
UHF sum, HS5
UHF step, HS6
UHF oscillator, HS7.

10.3 OUTPUT BOX ASSEMBLY OB

a) The range divider circuit board (RD) is also housed in a fully screened RF enclosure and is divided into 4 sections listed below:

Range divider, RD1
UHF oscillator, RD2
Down converter, RD3
Output control, RD4.

NB The output amplifier, OA, is an integral part of the range divider circuit board.



ASSEMBLY & BOARD LOCATION
DIAGRAM 4ZU10050220 ISS-A

FARNELL INSTRUMENTS LTD.

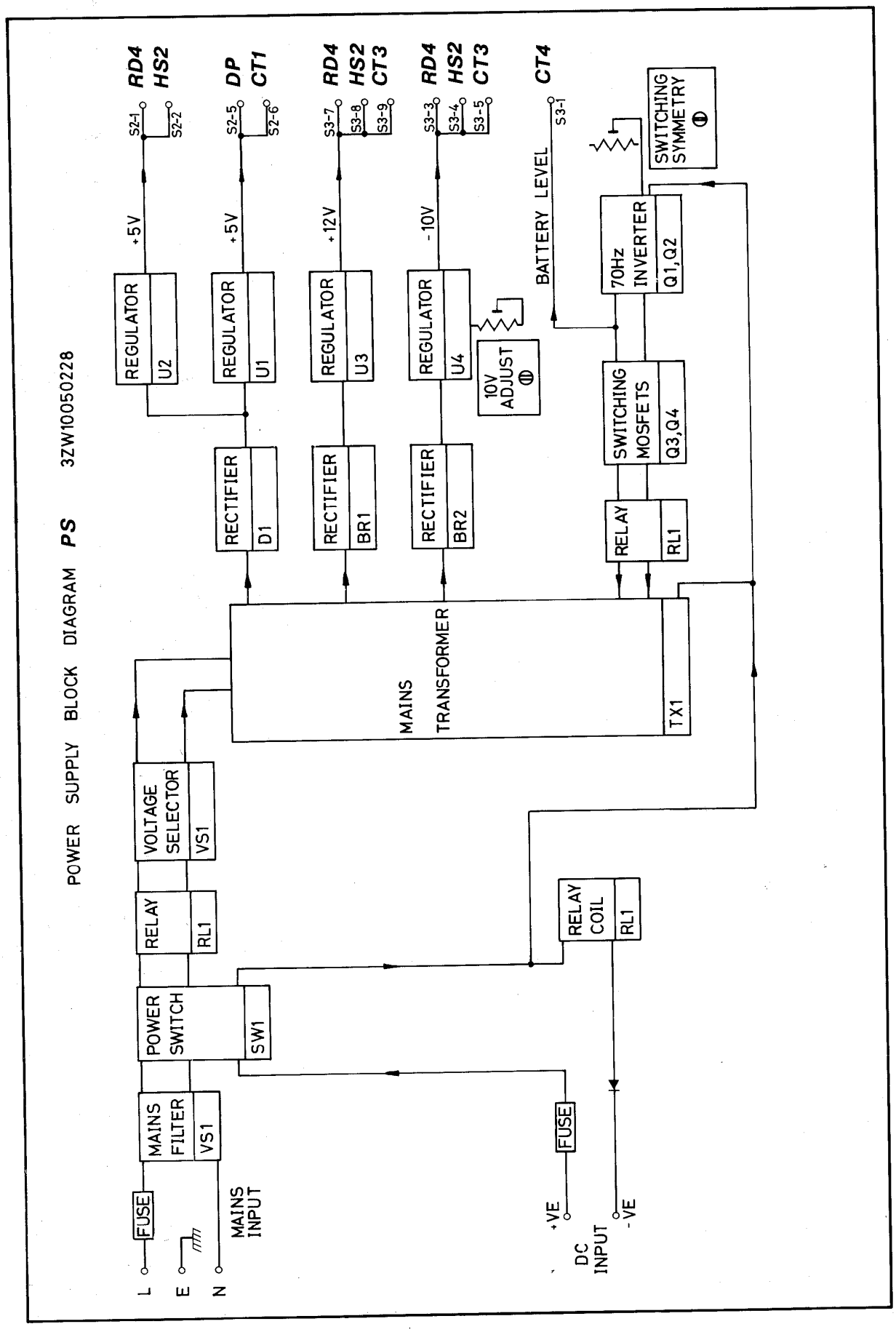
	TYPE PSG1000	COMPUTER No.	Sht 6 of 6 Shts	UK 10050

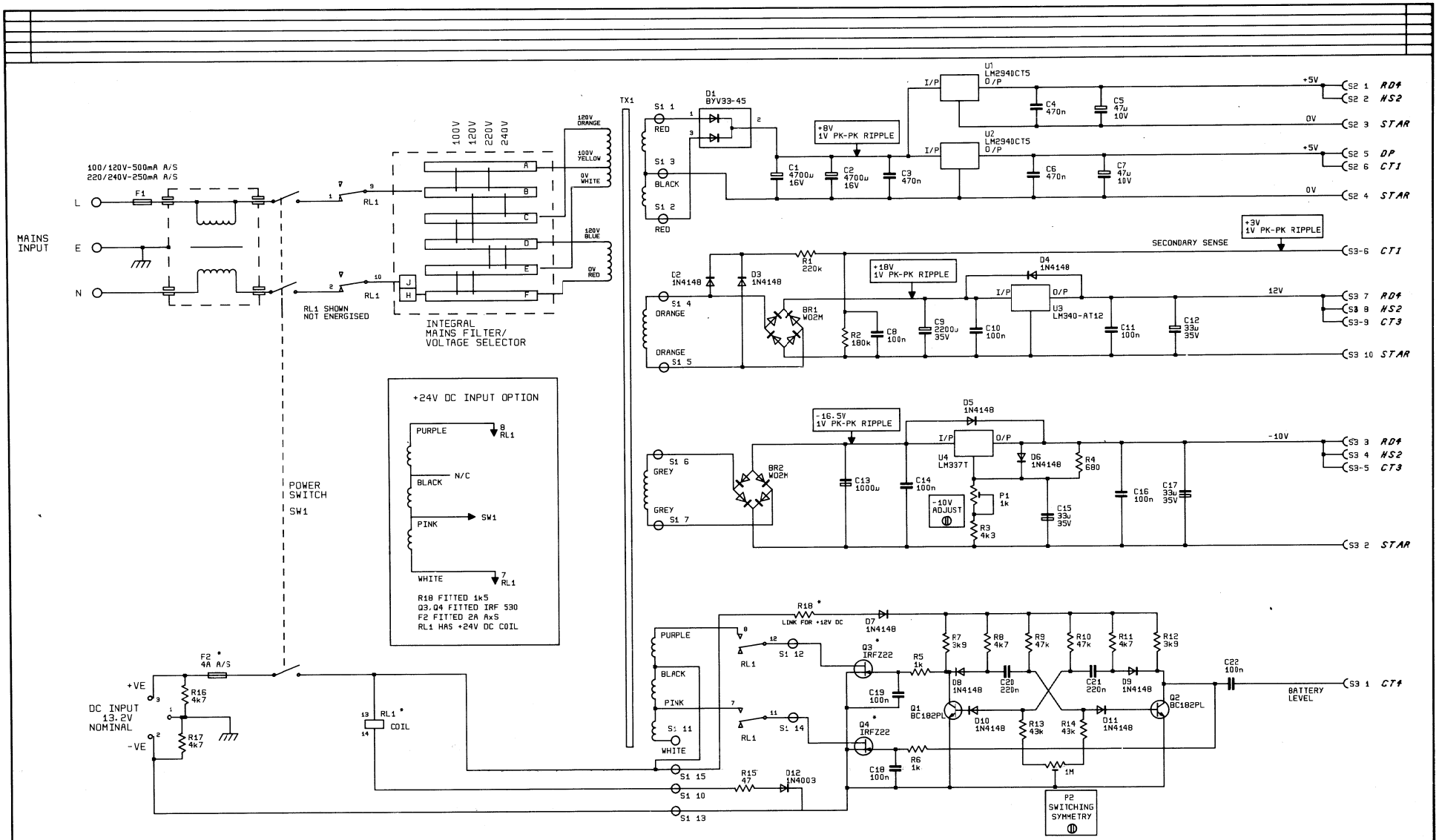
	DRAWING No.	COMPUTER No.	DESCRIPTION	QTY	ISS	MODIFICATION REF
1	CZX10050 204	SHT 1	CONTROL BD CCT DIAG CT1	REF	B	1
2	"	SHT 2	" CT2	"	A	
3	"	SHT 3	" CT3	"	A	
4	"	SHT 4	" CT4	"	B	1
5	CZX10050202	SHT 1	R.D. BD CCT DIAG RD1,2	"	B	1
6	"	SHT 2	" RD3	"	B	1
7	"	SHT 3	" RD4	"	B	1
8	CZX10050203		O/P AMP CCT DIAG OA	"	B	1
9	CZX10050201		P/S CCT DIAG PS	"	B	
10	RSZX0322		SYNTH BD CCT DIAG HS	"	A	
11	CZX10050206		DISP BD CCT DIAG DP	"	A	
12	3ZX10050207		AUX BD CCT DIAG AX	"	A	
13						
14						
15	3ZW10050210		OVERALL BLOCK DIAG	REF	A	
16	4ZW10050220		BOARD LOCATION DIAG	"	A	
17	3ZW10050221		F/P CONTROLS DIAG	"	A	
18	4ZW10050222		B/P CONTROLS DIAG	"	A	
19	3ZW10050223		RANGE CONTROL BLOCK DIAG RD1,2	"	A	
20	4ZW10050224		DOWN CONVERTER BLOCK DIAG RD3	"	A	
21	CZW10050225		O/P CONTROL BLOCK DIA RD4	"	A	
22	CZW10050226		O/P AMP BLOCK DIAG OA	"	A	
23	CZW10050227		SINAD & METER DRIVE BLOCK DIAG CT4	"	A	
24	3ZW10050228		P/S BLOCK DIAG PS	"	A	
25	RZW10050229		CONTROL BLOCK DIA CT1	"	A	
	RZW10050230		AUDIO SYNTH BLOCK DIA CT2	"	A	
	RZW10050231		MODULATION CONTROL BLOCK DIA CT3	"	A	
	RZW10050232		SYNTH BLOCK DIAG HS	"	A	
	RZW10050233		DISP BLOCK DIAG DP	"	A	
	RZW10050234		COMP STRUCTURE DIAG	"	A	

REF	1	2	3	4	5	6	7	8	9	10
ISSUE	A									
DATE	24/2/87									
MOD	12542 12500 12593 12624									
DRAWN	11	12	13	14	15	16	17	18	19	20
DATE										

FIUK

GAF 5717/79


POWER SUPPLY BLOCK DIAGRAM PS 3ZW10050228
L
E
N
MAINS INPUT
FUSE
MAINS FILTER
VS1
POWER SWITCH
SW1
RELAY
RL1
VOLTAGE SELECTOR
VS1
MAINS TRANSFORMER
TX1
RECTIFIER
D1
RECTIFIER
BR1
RECTIFIER
BR2
REGULATOR
U2
REGULATOR
U1
REGULATOR
U3
REGULATOR
U4
+5V
+5V
+12V
-10V
RD4
HS2
DP
CT1
RD4
HS2
CT3
RD4
HS2
CT3
S2-1
S2-2
S2-5
S2-6
S3-7
S3-8
S3-9
S3-3
S3-4
S3-5
10V ADJUST
BATTERY LEVEL
CT4
S3-1
70Hz INVERTER
Q1,Q2
SWITCHING MOSFETS
Q3,Q4
RELAY
RL1
SWITCHING SYMMETRY
RELAY COIL
RL1
FUSE
+VE
-VE
DC INPUT



ISS	A	B									
DATE	17/4/86	16/1/87									
MOD. NO.											
CHK'D		S.D									
NAME	J.C	H.D									

USED ON: F10050-PSG1000.

NOTES: ALL CAPACITOR VALUES IN F. ALL RESISTOR VALUES IN OHMS.
* SEE TABLE FOR +24V DC OPTION
UNLESS OTHERWISE STATED

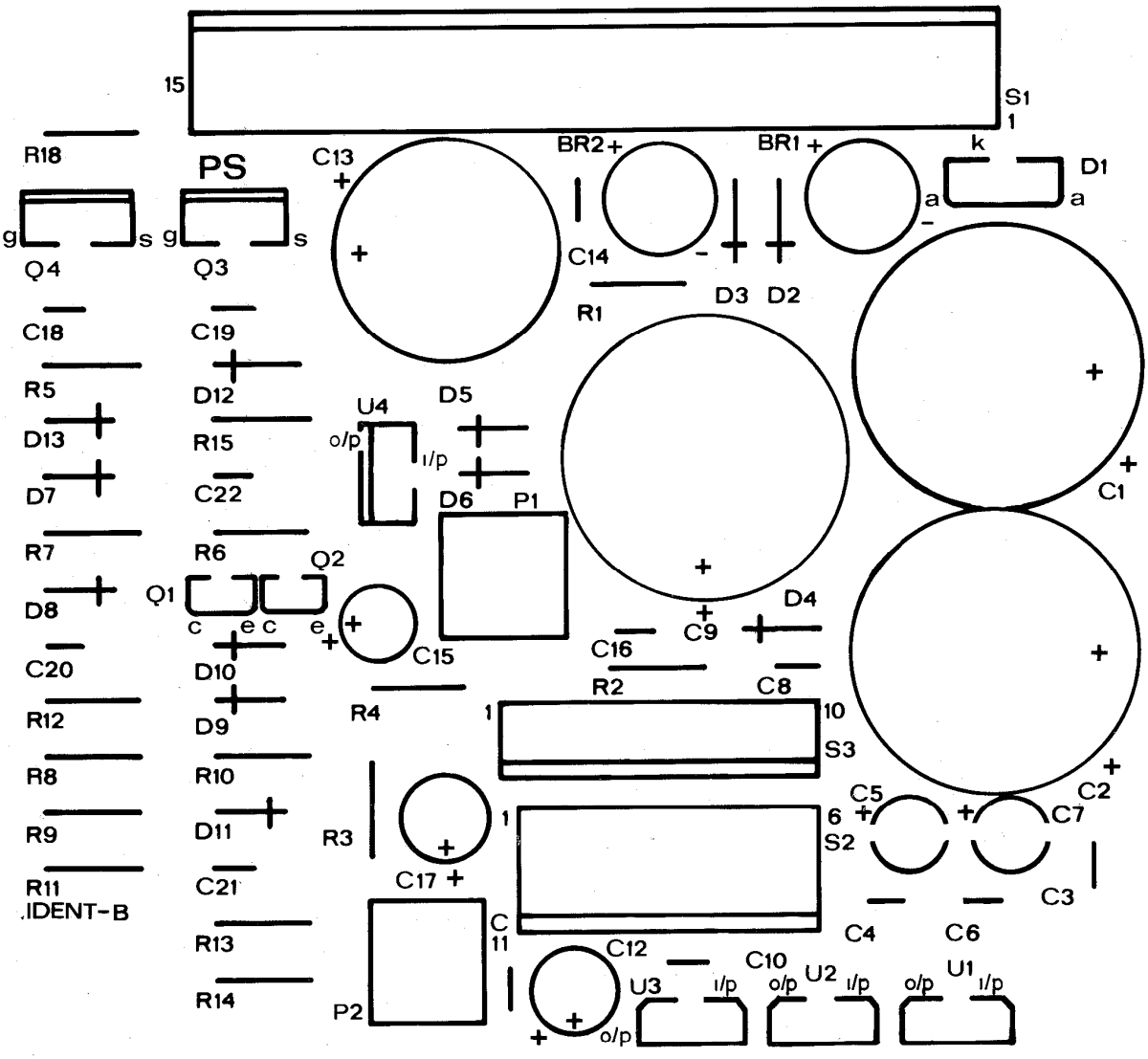
FARNELL INSTRUMENTS LTD.,

TITLE: POWER SUPPLY CIRCUIT DIAGRAM

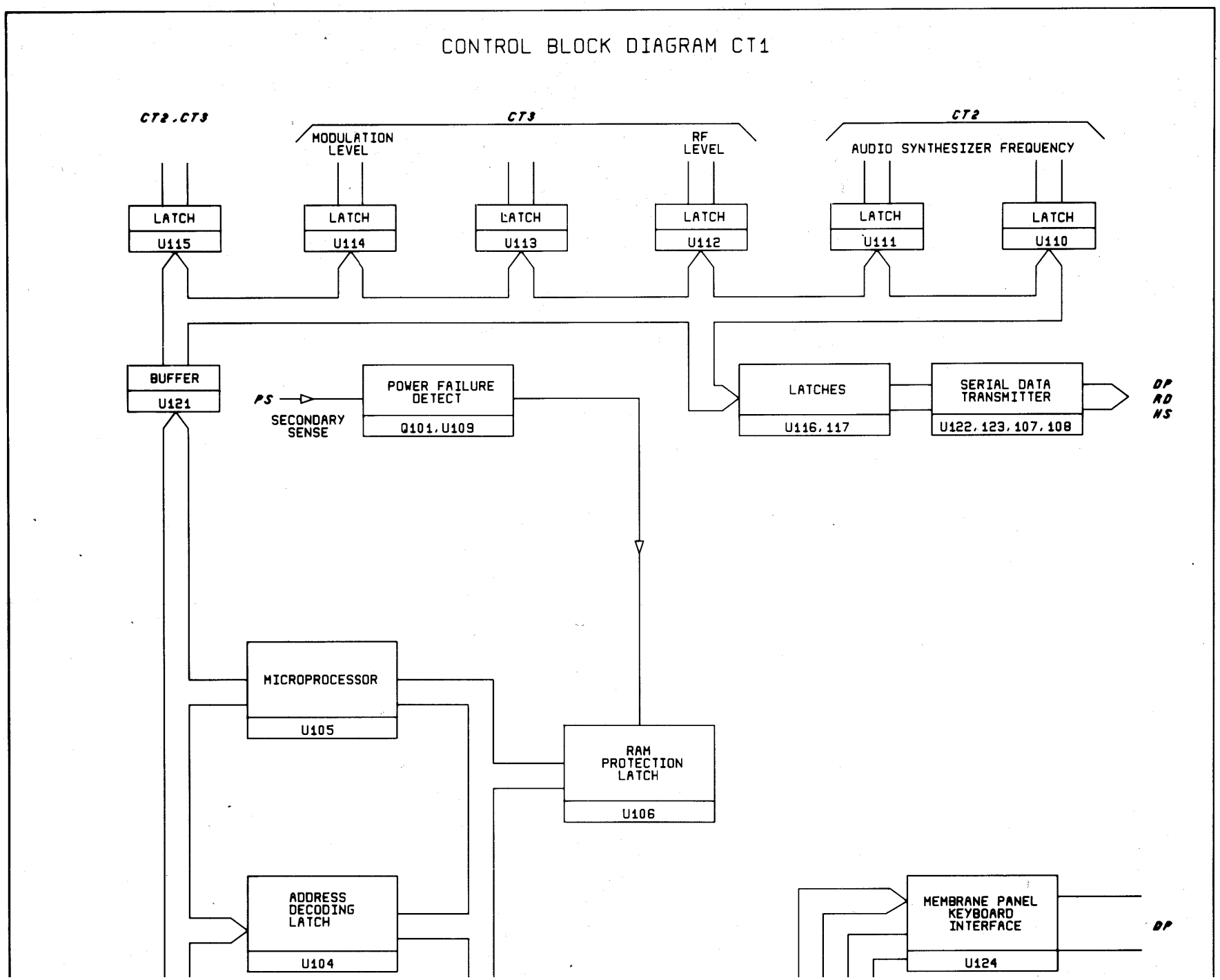
DRAWING NO. CZX10050201

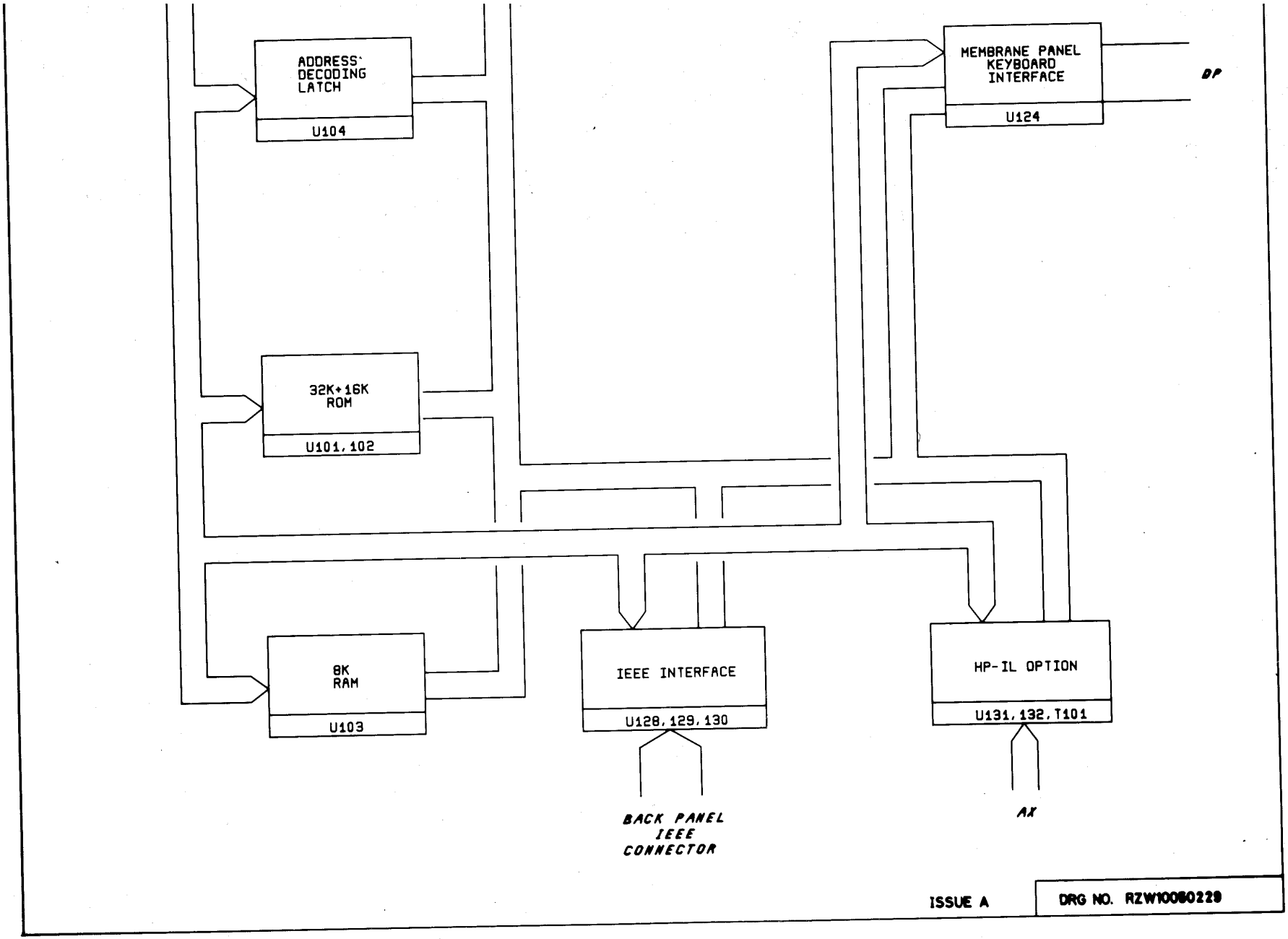
SHEET OF SHEETS

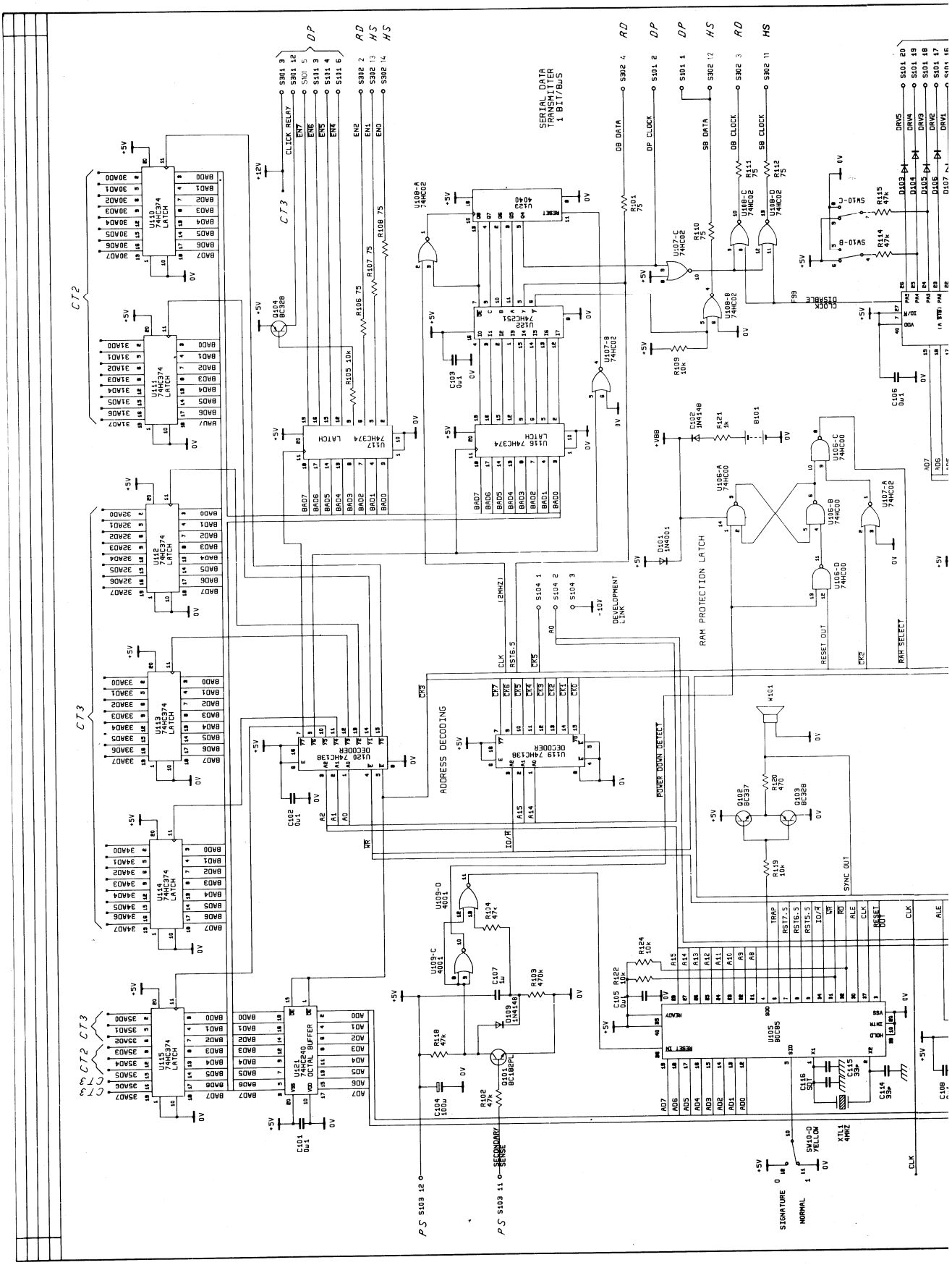
POWER SUPPLY COMPONENT LOCATION

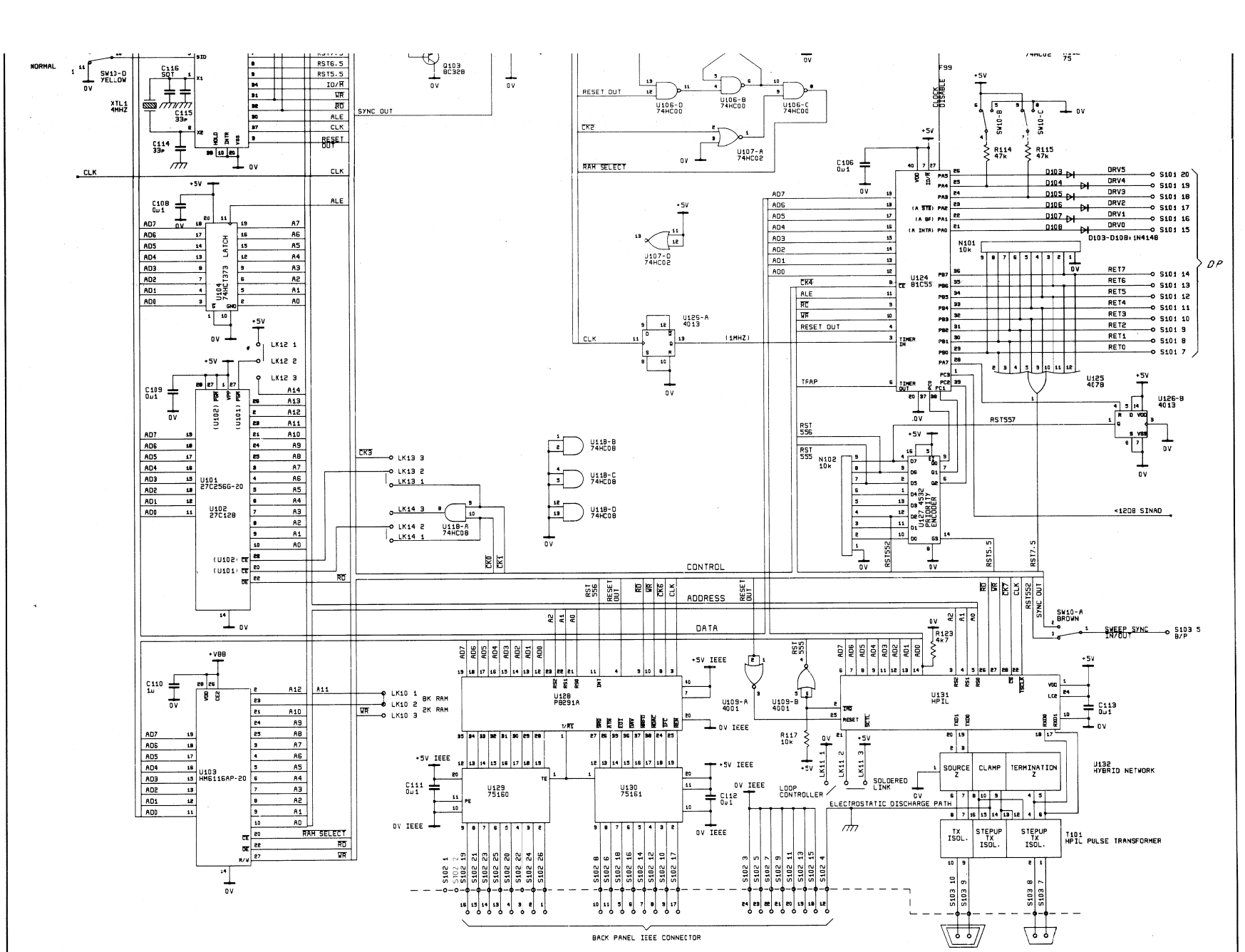


CONTROL BLOCK DIAGRAM CT1




ADDRESS DECODING LATCH
U104
MEMBRANE PANEL KEYBOARD INTERFACE
U124
DP
32K+16K ROM
U101, 102
8K RAM
U103
IEEE INTERFACE
U128, 129, 130
HP-IL OPTION
U131, 132, T101
BACK PANEL IEEE CONNECTOR
AX
ISSUE A
DRG NO. RZW10080220


SERIAL DATA TRANSMITTER 1 BIT/BUS
DB DATA
DP CLOCK
SB DATA
DB CLOCK
SB CLOCK
CLICK RELAY
RAM PROTECTION LATCH
ADDRESS DECODING
POWER DOWN DETECT
DEVELOPMENT LINK
RESET OUT
RAM SELECT
SYNC OUT
SIGNATURE
NORMAL
SECONDARY SENSE
CLOCK DISABLE



ISS	A	B
DATE	16/10/86	17/2/87
ECO. NO.		12500
CHK'D	SR	SR
DRWN	JEC	JEC

USED ON: PSG1000 F10050

NOTES: ALL CAPACITOR VALUES IN F. ALL RESISTOR VALUES IN OHMS.

UNLESS OTHERWISE STATED

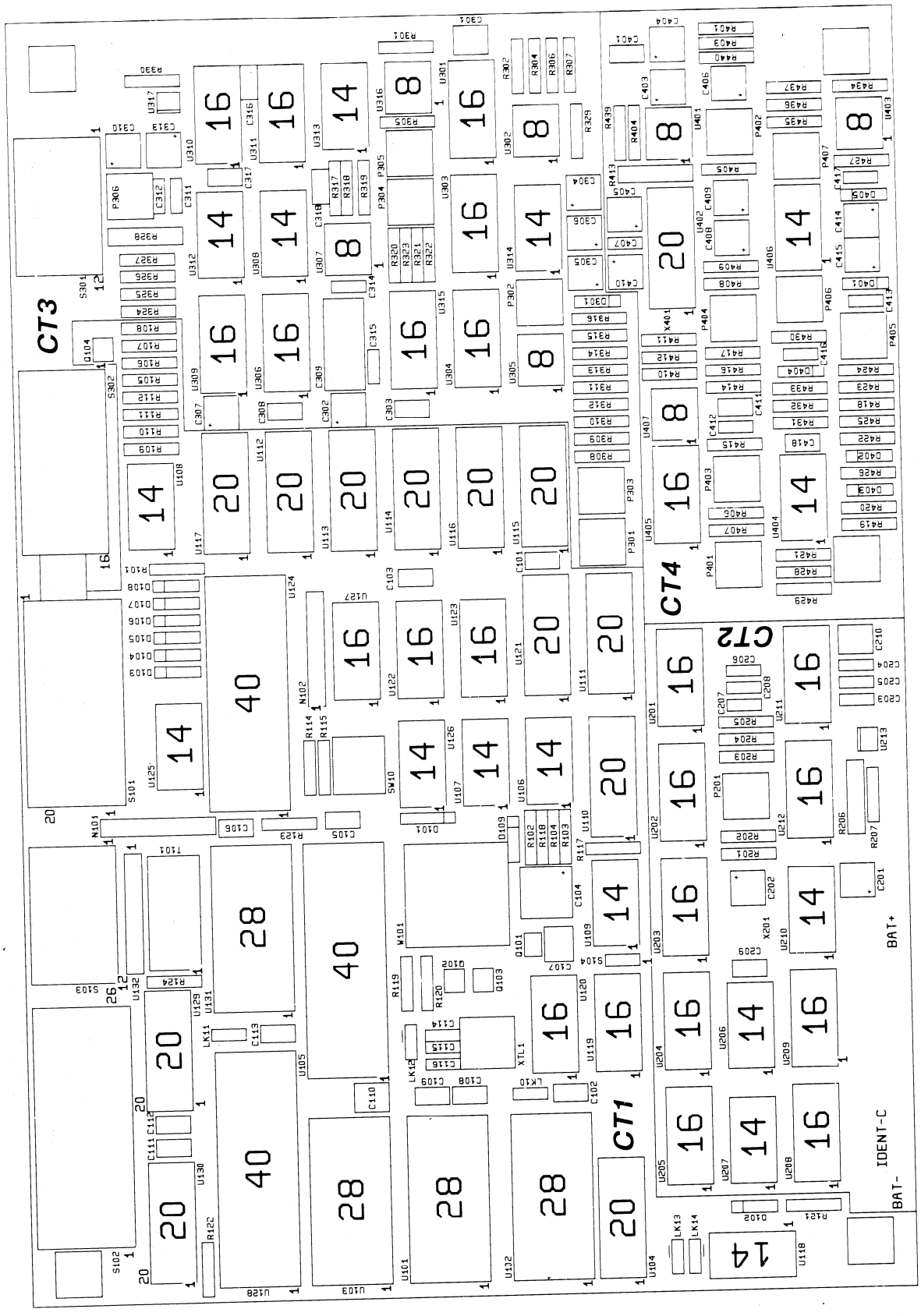
FARNELL INSTRUMENTS LTD., SANDBECK WAY, WETHERBY, YORKS. LS22 4DH

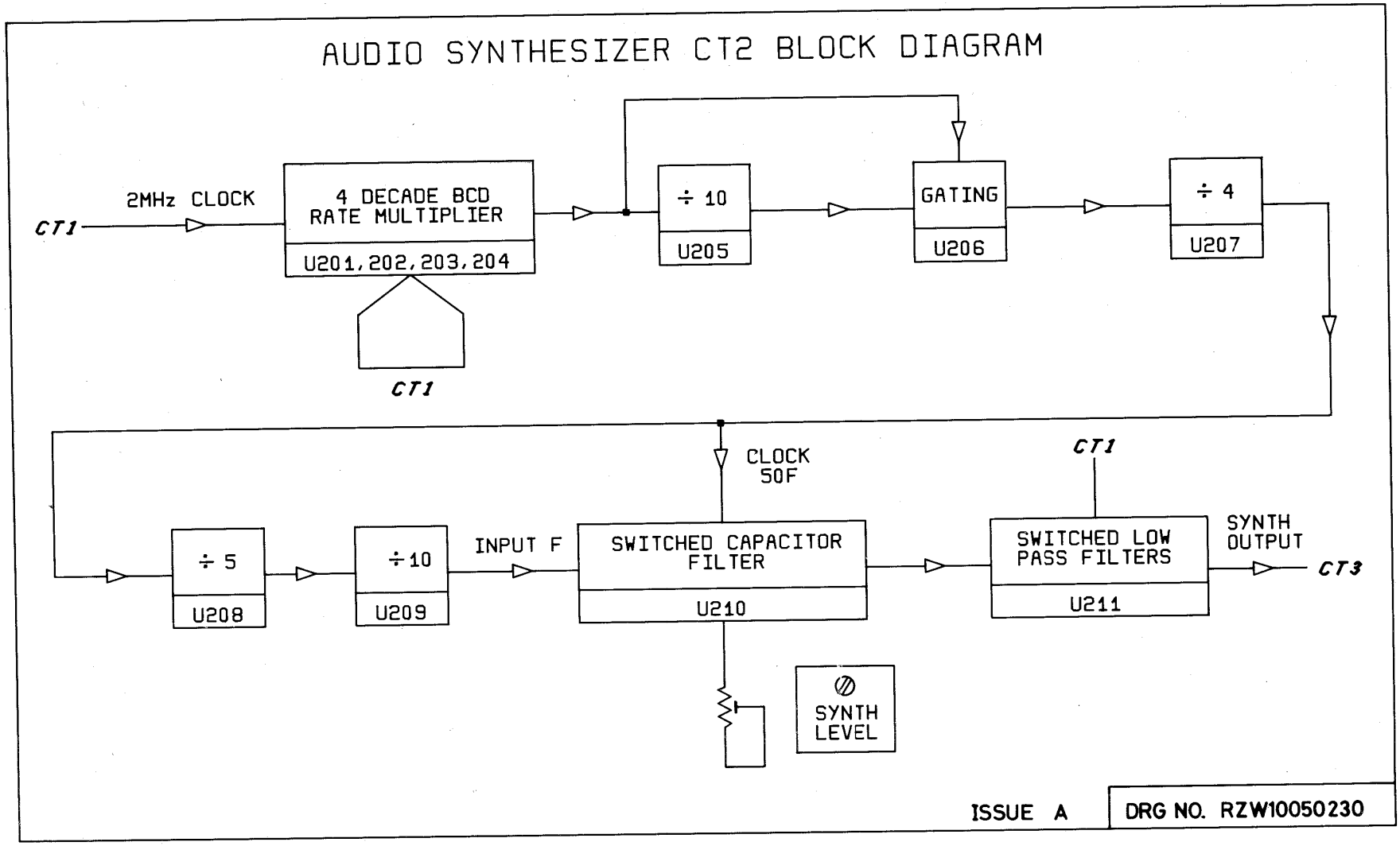
TITLE: CONTROL BOARD CIRCUIT DIAGRAM
CT1 CONTROL SECTION

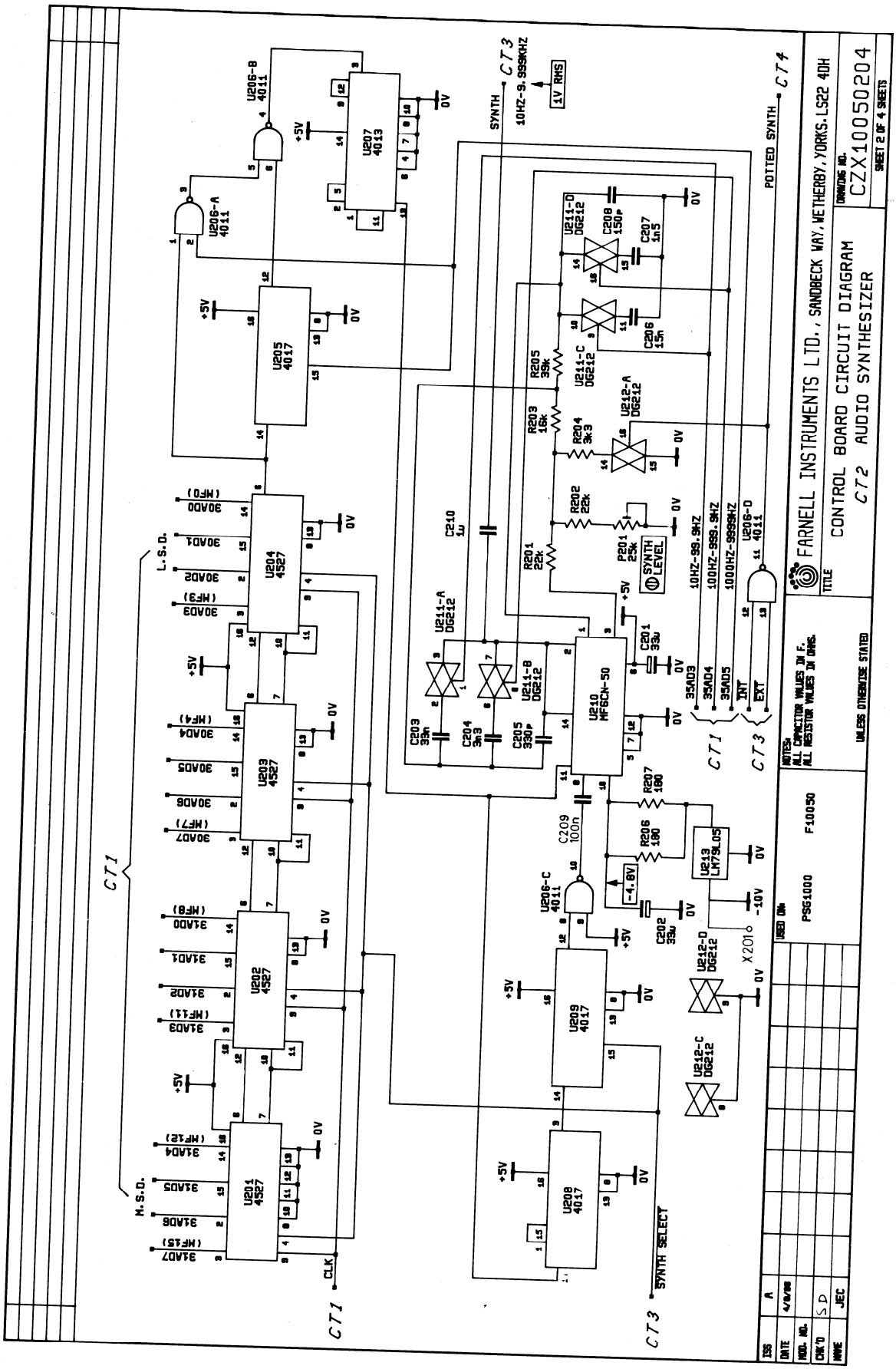
DRAWING NO. CZX10050204

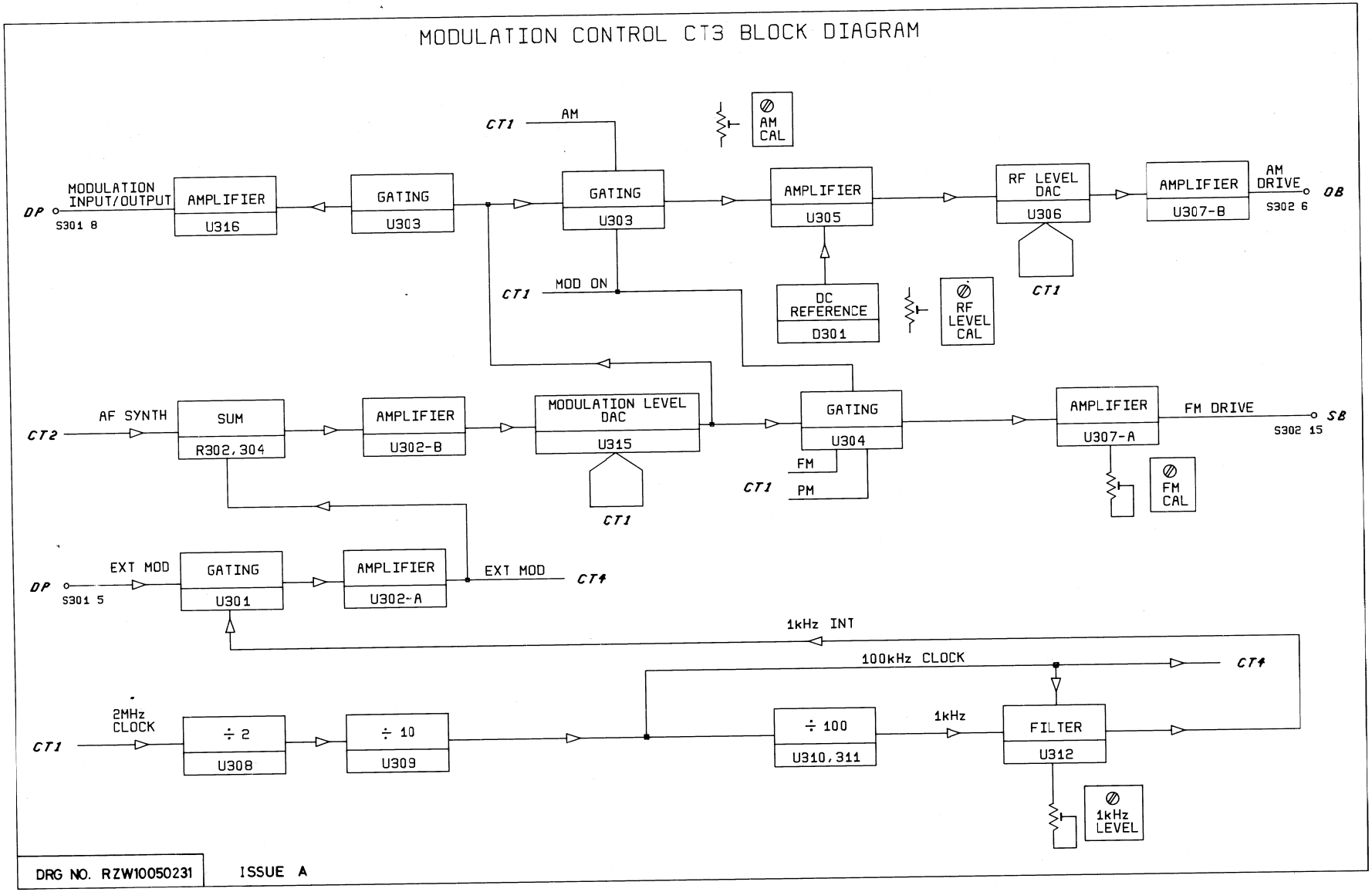
SHEET 1 OF 4 SHEETS

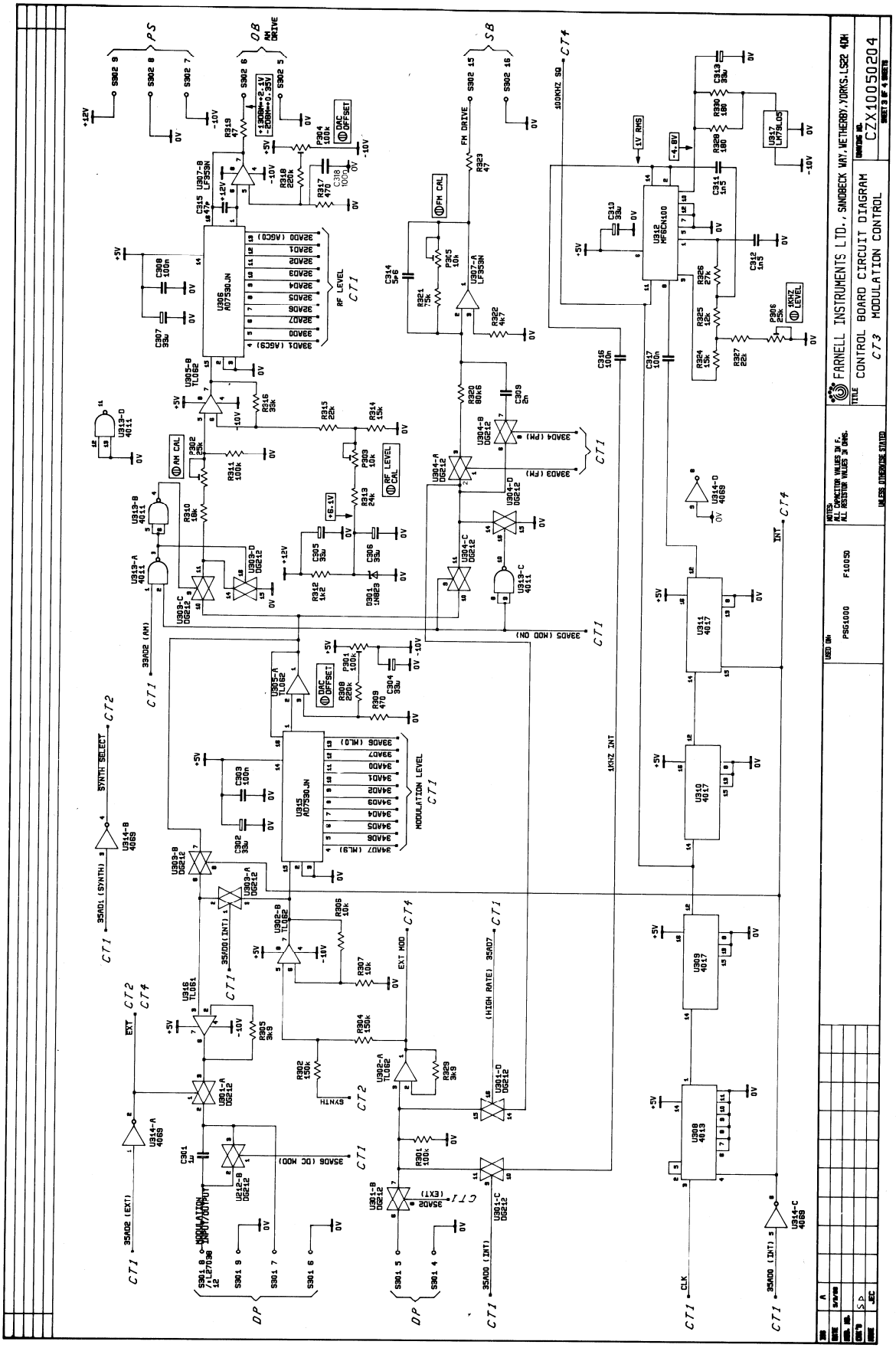
CONTROL COMPONENT LOCATION



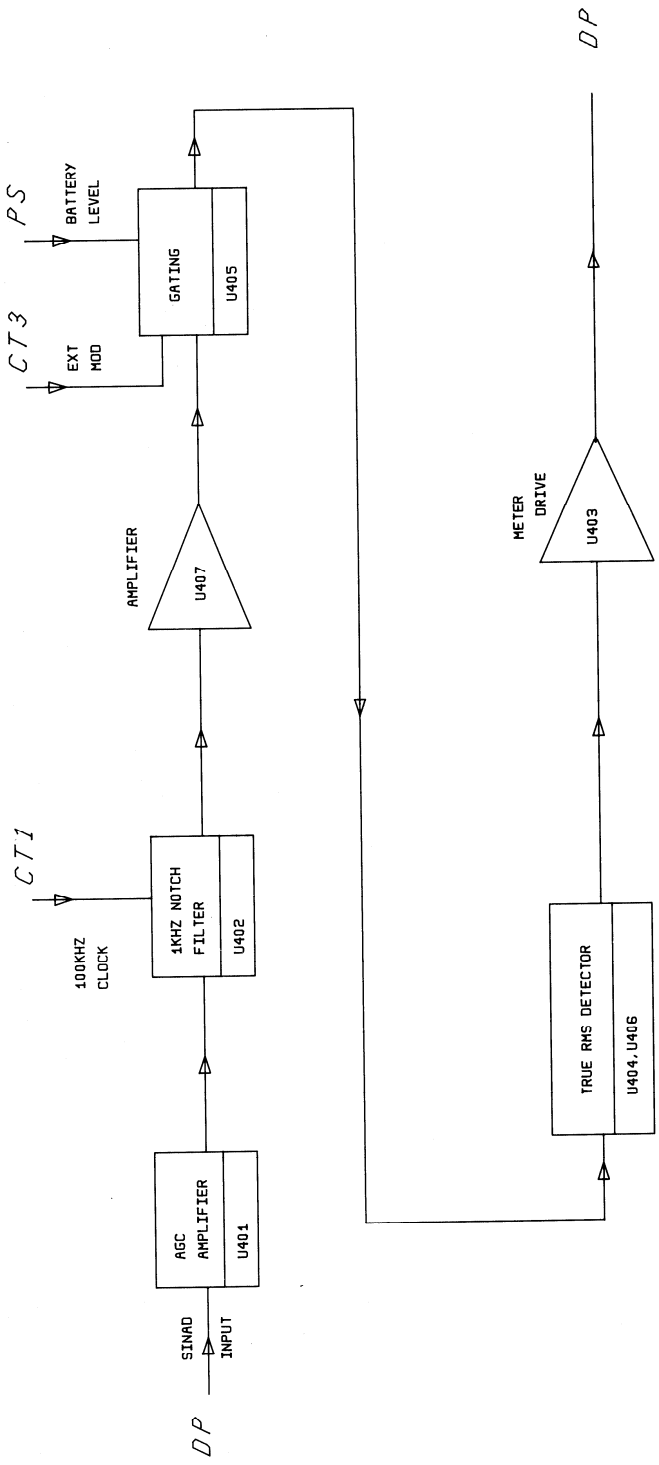

AUDIO SYNTHESIZER CT2 BLOCK DIAGRAM
CT1
2MHz CLOCK
4 DECADE BCD RATE MULTIPLIER
U201,202,203,204
CT1
÷ 10
U205
GATING
U206
÷ 4
U207
CLOCK 50F
CT1
÷ 5
U208
÷10
U209
INPUT F
SWITCHED CAPACITOR FILTER
U210
SWITCHED LOW PASS FILTERS
U211
SYNTH OUTPUT
CT3
SYNTH LEVEL
ISSUE A
DRG NO. RZW10050230

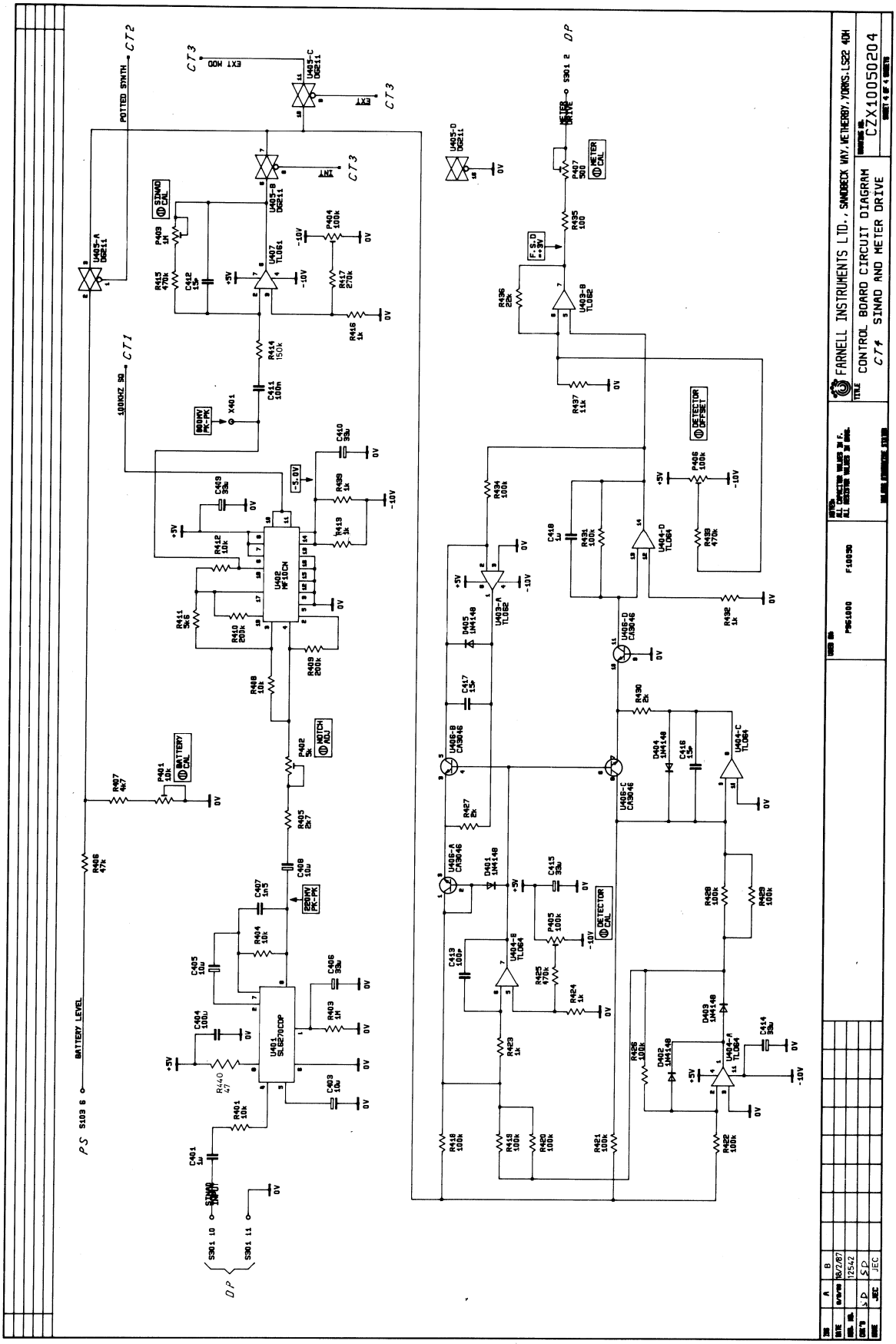

FARNELL INSTRUMENTS LTD., SANDBECK WAY, WETHERBY, YORKS. LS22 4DH
TITLE
CONTROL BOARD CIRCUIT DIAGRAM
CT2 AUDIO SYNTHESIZER
DRAWING NO.
CZX10050204
SHEET 2 OF 4 SHEETS
NOTES: ALL CAPACITOR VALUES IN F. ALL RESISTOR VALUES IN OHMS.
UNLESS OTHERWISE STATED
USED ON
PSG1000
F10050
ISS
DATE
MODL. NO.
CHK'D
NAME
SYNTH
10HZ-9.999KHZ
1V RMS
POTTED SYNTH
SYNTH SELECT
CLK
L.S.D.
M.S.D.
10HZ-99.9HZ
100HZ-999.9HZ
1000HZ-9999HZ
SYNTH LEVEL
INT
EXT
-4.8V
-10V
X2016
U201 4527
U202 4527
U203 4527
U204 4527
U205 4017
U206-A 4011
U206-B 4011
U206-C 4011
U206-D 4011
U207 4013
U208 4017
U209 4017
U210 HF6CN-50
U211-A DG212
U211-B DG212
U211-C DG212
U211-D DG212
U212-A DG212
U212-C DG212
U212-D DG212
U213 LM79L05
R201 22k
R202 22k
R203 16k
R204 3k3
R205 39k
R206 180
R207 180
P201 25k
C201 33u
C202 33u
C203 33n
C204 3n3
C205 330p
C206 15n
C207 1n5
C208 150p
C209 100n
C210 1u

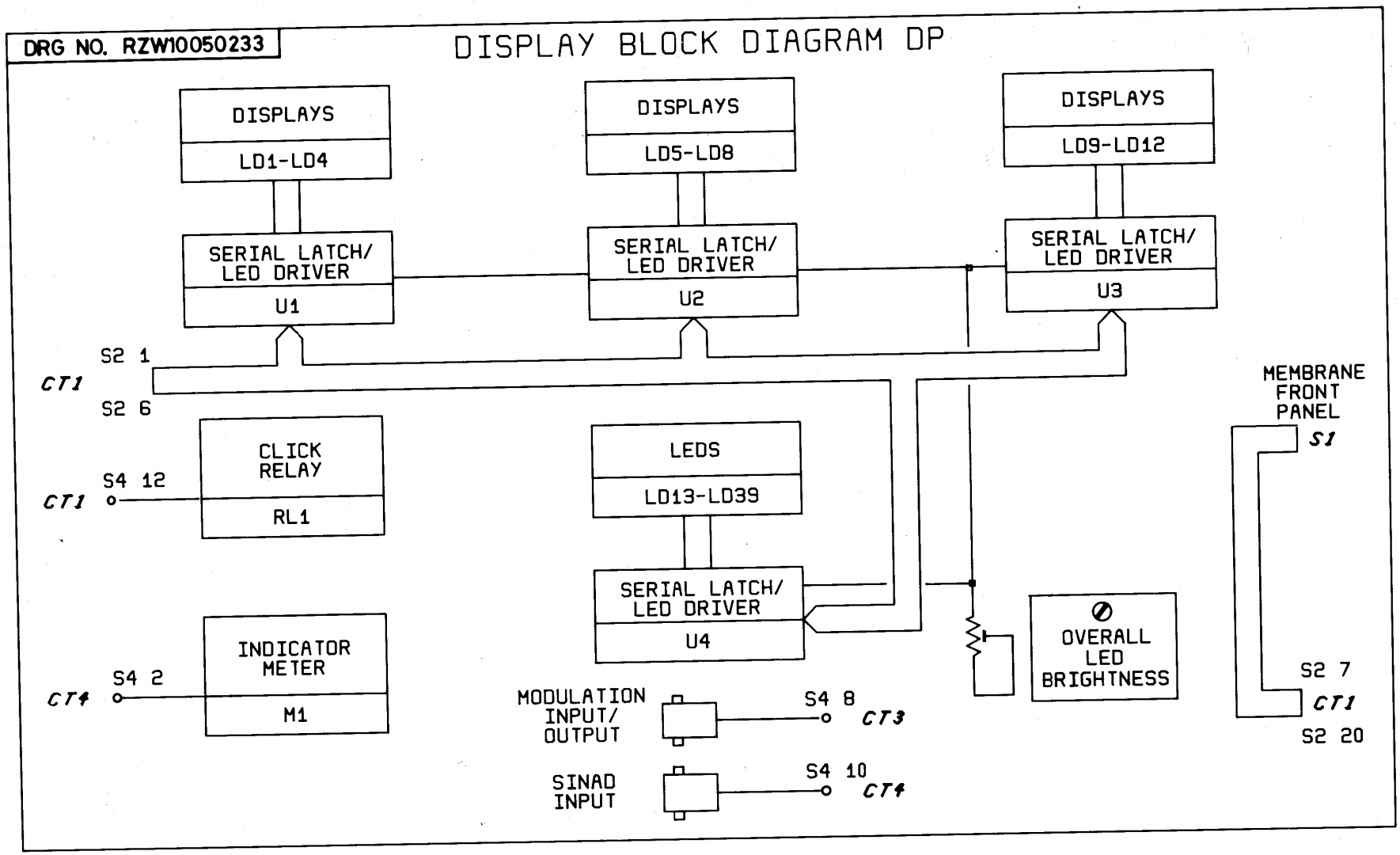

MODULATION CONTROL CT3 BLOCK DIAGRAM
CT1
AM
AM CAL
MODULATION INPUT/OUTPUT
DP
S301 8
AMPLIFIER
U316
GATING
U303
GATING
U303
AMPLIFIER
U305
RF LEVEL DAC
U306
AMPLIFIER
U307-B
AM DRIVE
S302 6
OB
CT1
MOD ON
DC REFERENCE
D301
RF LEVEL CAL
CT1
AF SYNTH
CT2
SUM
R302,304
AMPLIFIER
U302-B
MODULATION LEVEL DAC
U315
CT1
GATING
U304
FM
PM
CT1
AMPLIFIER
U307-A
FM DRIVE
S302 15
SB
FM CAL
EXT MOD
DP
S301 5
GATING
U301
AMPLIFIER
U302-A
EXT MOD
CT4
1kHz INT
100kHz CLOCK
CT4
2MHz CLOCK
CT1
÷ 2
U308
÷ 10
U309
÷ 100
U310,311
1kHz
FILTER
U312
1kHz LEVEL
DRG NO. RZW10050231
ISSUE A

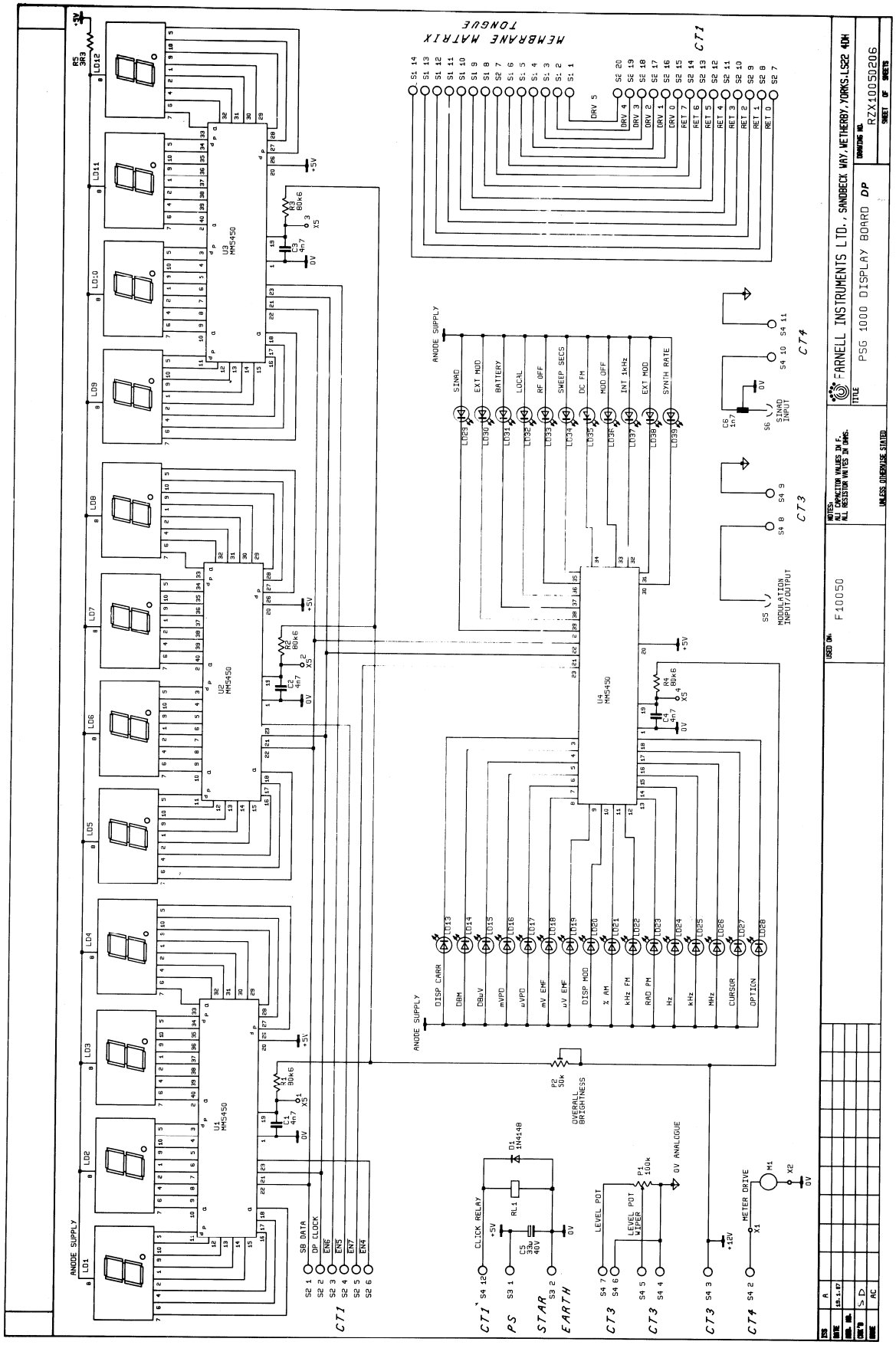

FARNELL INSTRUMENTS LTD., SANDBECK WAY, WETHERBY, YORKS. LS22 4DH
CONTROL BOARD CIRCUIT DIAGRAM
C73 MODULATION CONTROL
CZX10050204
PS61000
F10050
AM CAL
FM CAL
RF LEVEL CAL
DAC OFFSET
AM DRIVE
FM DRIVE
RF LEVEL
MODULATION LEVEL
SYNTH SELECT
EXT MOD
1KHZ LEVEL
LV RMS
100KHZ SQ
1KHZ INT
MODULATION INPUT/OUTPUT
AD7590JN
TL082
DG212
4011
4066
4017
4013
MF6CN100
LF353N
LF79L05

SINAD AND METER DRIVE BLOCK DIAGRAM CT4 CZW10050227 ISS.A

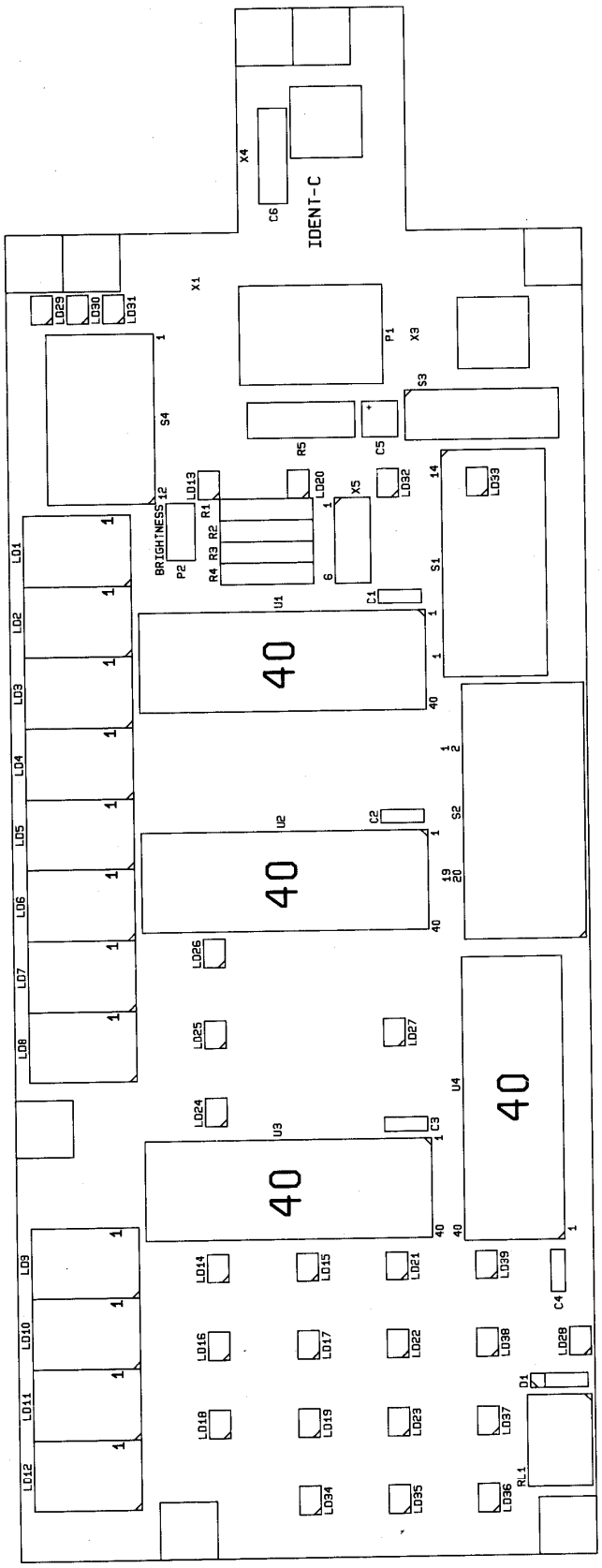


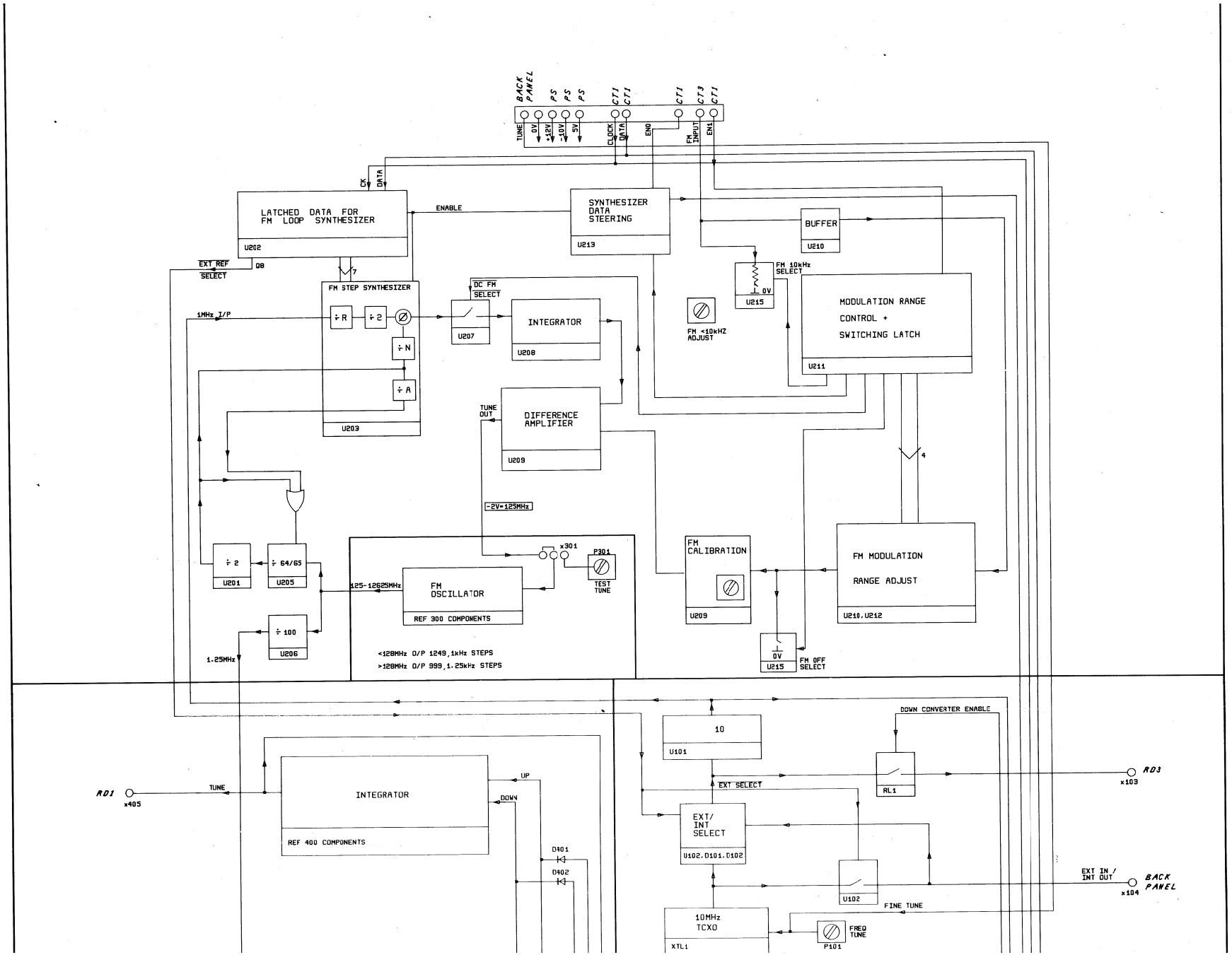

FARNELL INSTRUMENTS LTD., SANDBECK WAY, WETHERBY, YORKS. LS22 4DH
CONTROL BOARD CIRCUIT DIAGRAM
CT4 SINAD AND METER DRIVE
CZX10050204
F10030
P961000
POTTED SYNTH
CT1
CT2
CT3
CT4
EXT MOD
100KHZ SQ
BATTERY LEVEL
PS S103 6
DP S301 2
S301 10
S301 11
METER DRIVE
F.S.D +-8V
SINAD CAL
BATTERY CAL
NOTCH ADJ
METER CAL
DETECTOR CAL
DETECTOR OFFSET
-5.0V
X401
U401 SL627/NCOP
U402 MF10CN
U403-A TL082
U403-B TL082
U404-A TL064
U404-B TL064
U404-C TL064
U404-D TL064
U405-A DG211
U405-B DG211
U405-C DG211
U405-D DG211
U406-A CA3046
U406-B CA3046
U406-C CA3046
U406-D CA3046

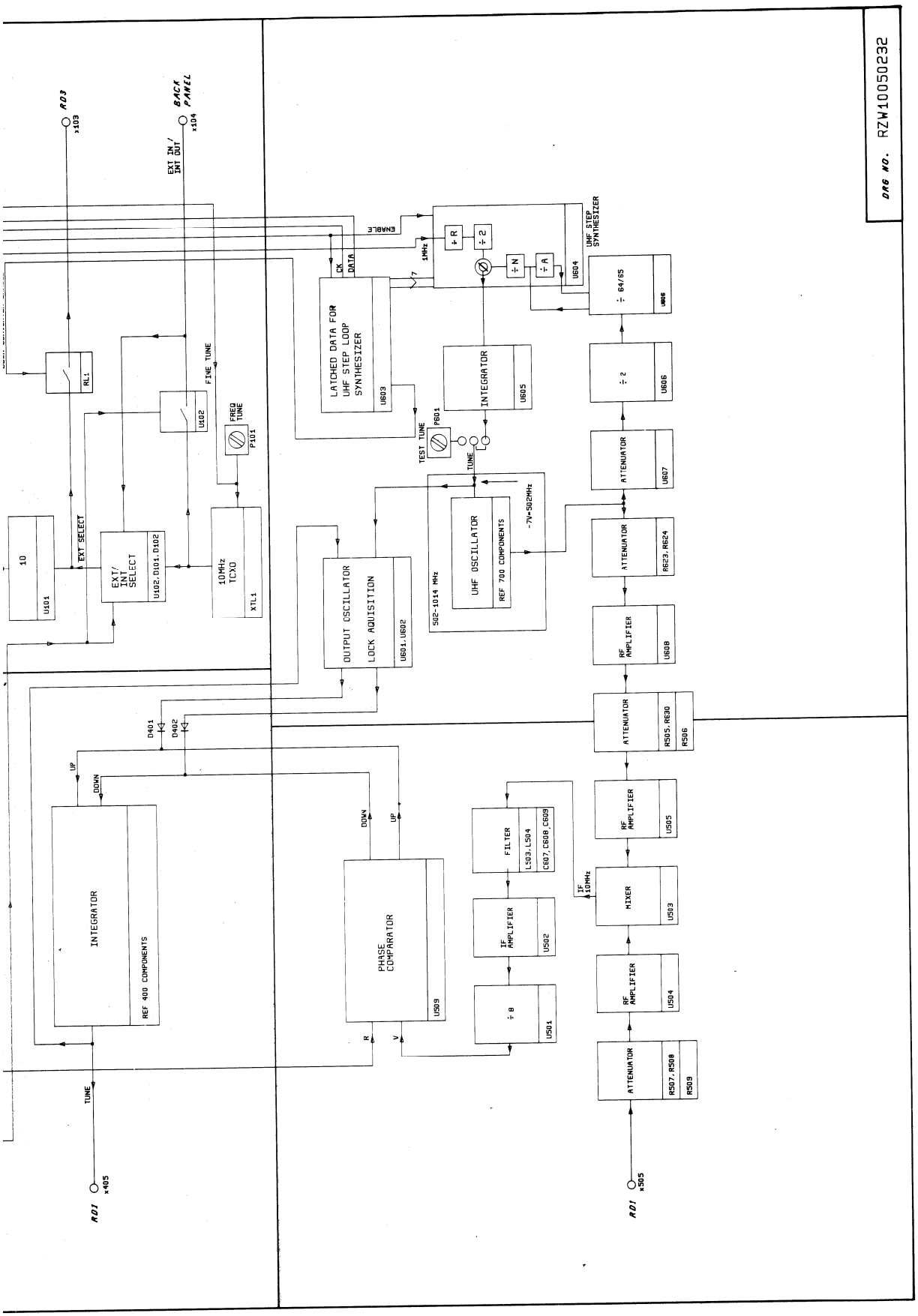

DRG NO. RZW10050233
DISPLAY BLOCK DIAGRAM DP
DISPLAYS
LD1-LD4
DISPLAYS
LD5-LD8
DISPLAYS
LD9-LD12
SERIAL LATCH/
LED DRIVER
U1
SERIAL LATCH/
LED DRIVER
U2
SERIAL LATCH/
LED DRIVER
U3
S2 1
CT1
S2 6
CLICK
RELAY
RL1
S4 12
CT1
LEDS
LD13-LD39
SERIAL LATCH/
LED DRIVER
U4
INDICATOR
METER
M1
S4 2
CT4
MODULATION
INPUT/
OUTPUT
S4 8
CT3
SINAD
INPUT
S4 10
CT4
OVERALL
LED
BRIGHTNESS
MEMBRANE
FRONT
PANEL
S1
S2 7
CT1
S2 20

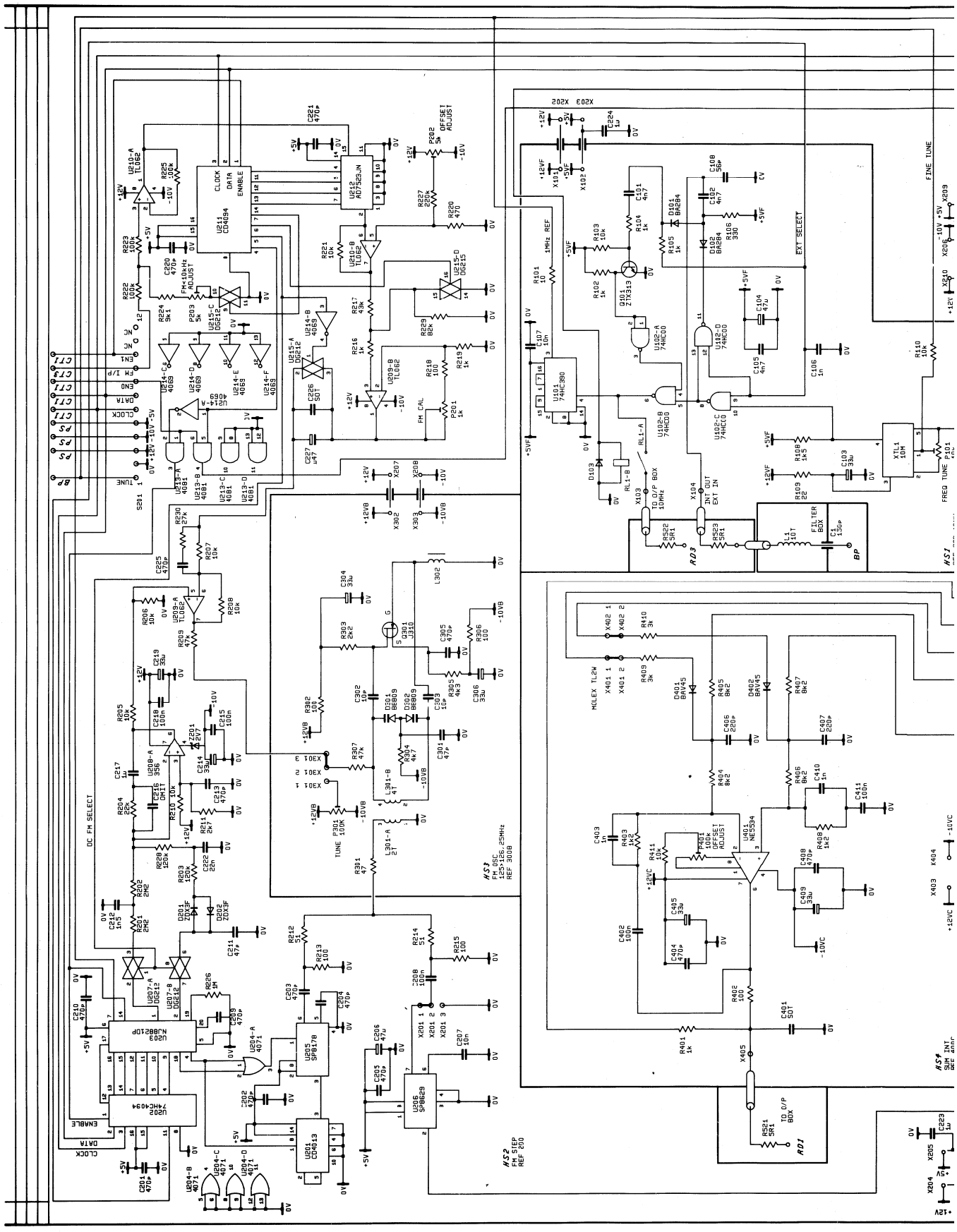

MEMBRANE MATRIX TONGUE
FARNELL INSTRUMENTS LTD., SANDBECK WAY, WETHERBY, YORKS. LS22 4DN
PSG 1000 DISPLAY BOARD DP
RZX1005020G
F10050
ANODE SUPPLY
SINAD
EXT MOD
BATTERY
LOCAL
RF OFF
SWEEP SECS
DC FM
MOD OFF
INT 1kHz
EXT MOD
SYNTH RATE
DISP CARR
DBM
DBuV
mVPD
uVPD
mV EMF
uV EMF
DISP MOD
% AM
kHz FM
RAD PM
Hz
kHz
MHz
CURSOR
OPTION
CLICK RELAY
LEVEL POT
METER DRIVE
SINAD INPUT
MODULATION INPUT/OUTPUT
OVERALL BRIGHTNESS
0V ANALOGUE
SB DATA
DP CLOCK
EN6
EN5
EN7
EN4
CT1
CT3
CT4
PS
STAR
EARTH

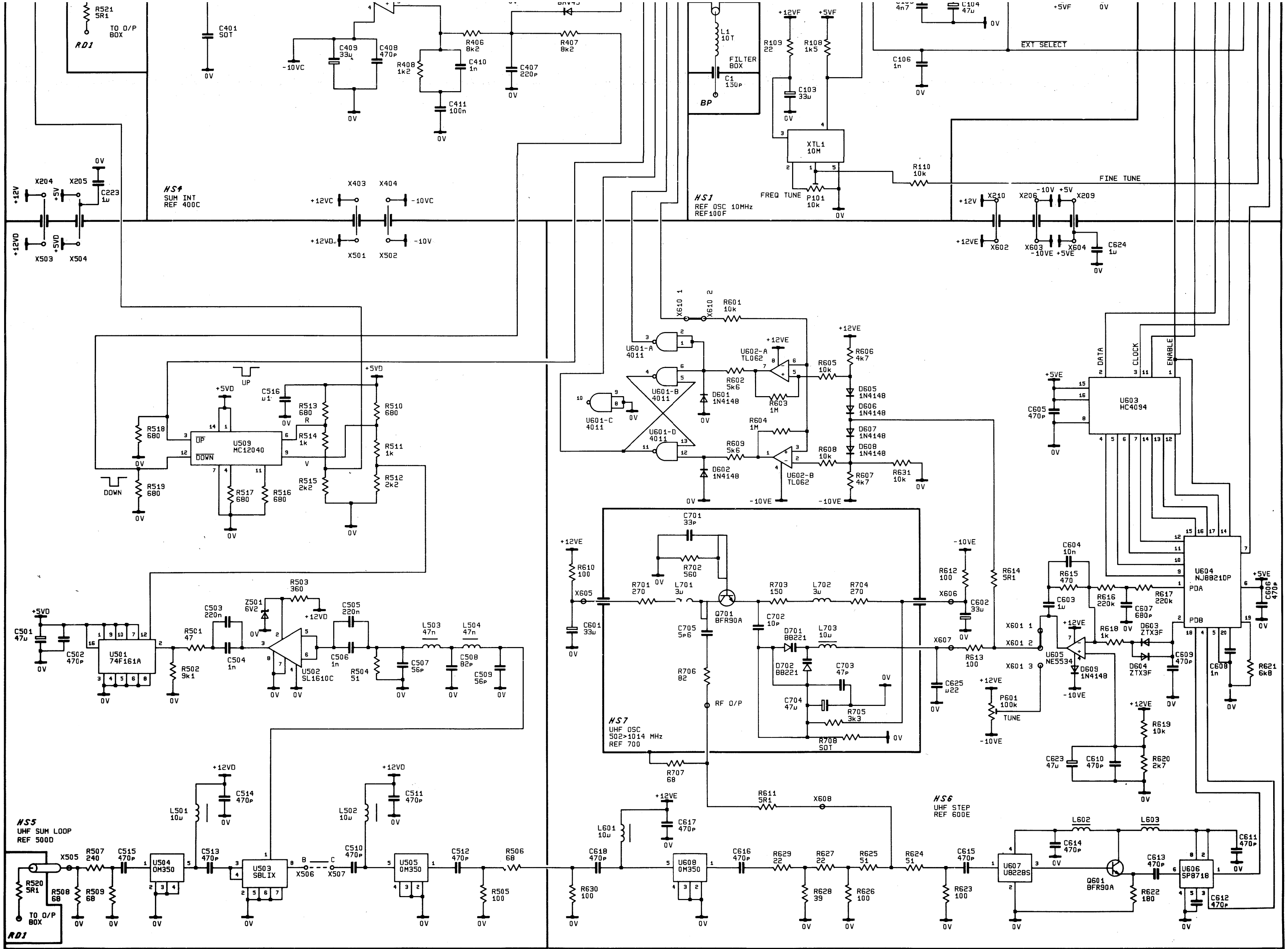
DISPLAY COMPONENT LOCATION




BACK PANEL
PS
PS
PS
CT1
CT1
CT1
CT3
CT1
TUNE
0V
+12V
-10V
5V
CLOCK
DATA
ENO
FM INPUT
EN1
CK
DATA
LATCHED DATA FOR FM LOOP SYNTHESIZER
U202
ENABLE
SYNTHESIZER DATA STEERING
U213
BUFFER
U210
EXT REF SELECT
D8
FM STEP SYNTHESIZER
÷ R
÷ 2
÷ N
÷ A
U203
1MHz I/P
DC FM SELECT
U207
INTEGRATOR
U208
FM 10kHz SELECT
0V
U215
FM <10kHZ ADJUST
MODULATION RANGE CONTROL + SWITCHING LATCH
U211
TUNE OUT
DIFFERENCE AMPLIFIER
U209
-2V=125MHz
÷ 2
U201
÷ 64/65
U205
÷ 100
U206
1.25MHz
125-128.25MHz
FM OSCILLATOR
REF 300 COMPONENTS
x301
P301
TEST TUNE
<128MHz O/P 1249,1kHz STEPS
>128MHz O/P 999,1.25kHz STEPS
FM CALIBRATION
U209
FM MODULATION RANGE ADJUST
U210.U212
0V
U215
FM OFF SELECT
DOWN CONVERTER ENABLE
10
U101
RD1
x405
TUNE
INTEGRATOR
REF 400 COMPONENTS
UP
DOWN
D401
D402
EXT SELECT
RL1
RD3
x103
EXT/ INT SELECT
U102,D101,D102
U102
FINE TUNE
EXT IN / INT OUT
x104
BACK PANEL
10MHz TCXO
XTL1
FREQ TUNE
P101


DRG NO. RZW10050232
RO3
x103
BACK PANEL
EXT IN/ INT OUT
x104
ENABLE
CK
DATA
1MHz
÷ R
÷ 2
÷ N
÷ A
UHF STEP SYNTHESIZER
U604
÷ 64/65
U606
÷ 2
U606
ATTENUATOR
U607
ATTENUATOR
R623, R624
RF AMPLIFIER
U608
ATTENUATOR
R505, R630
R506
RF AMPLIFIER
U505
MIXER
U503
RF AMPLIFIER
U504
ATTENUATOR
R507, R508
R509
RO1
x505
IF 10MHz
FILTER
L503-L504
C607, C608, C609
IF AMPLIFIER
U502
÷ 8
U501
PHASE COMPARATOR
U509
R
V
DOWN
UP
INTEGRATOR
REF 400 COMPONENTS
TUNE
RO1
x405
D401
D402
LATCHED DATA FOR UHF STEP LOOP SYNTHESIZER
U603
INTEGRATOR
U605
TEST TUNE
P601
TUNE
UHF OSCILLATOR
REF 700 COMPONENTS
-7V=502MHz
502-1014 MHz
OUTPUT OSCILLATOR
LOCK AQUISITION
U601, U602
FINE TUNE
FREQ TUNE
P101
U102
RL1
10MHz TCXO
XTL1
EXT/ INT SELECT
U102, D101, D102
EXT SELECT
10
U101





ISS	A
DATE	30.1.87
MOD. NO.	
CHK'D	DM
APPR'D	A.C

USED ON: F10050

NOTES:
ALL CAPACITOR VALUES IN F.
ALL RESISTOR VALUES IN OHMS.
UNLESS OTHERWISE STATED

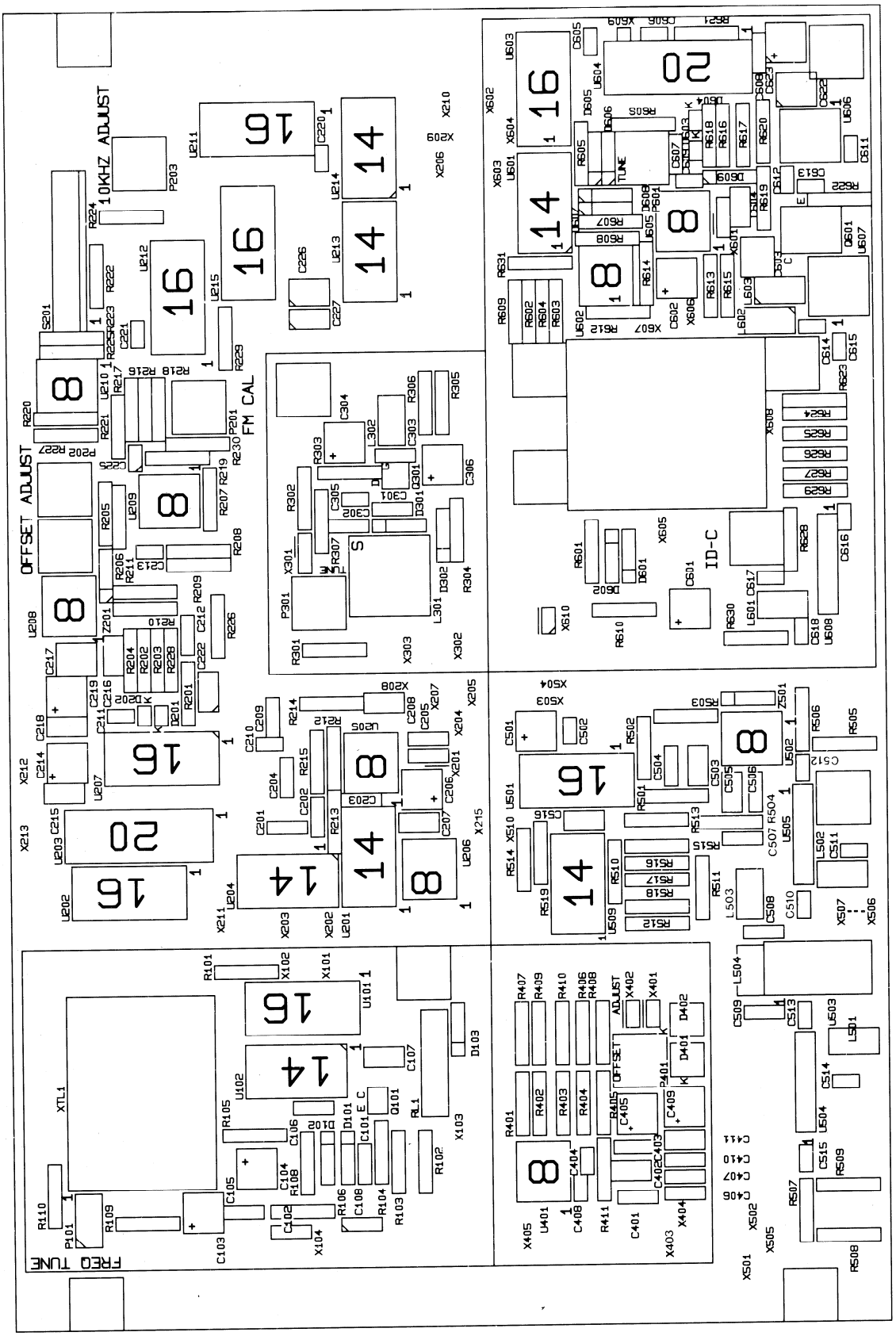
FARNELL INSTRUMENTS LTD.,

TITLE
PSG1000 SYNTH BD DIA HS

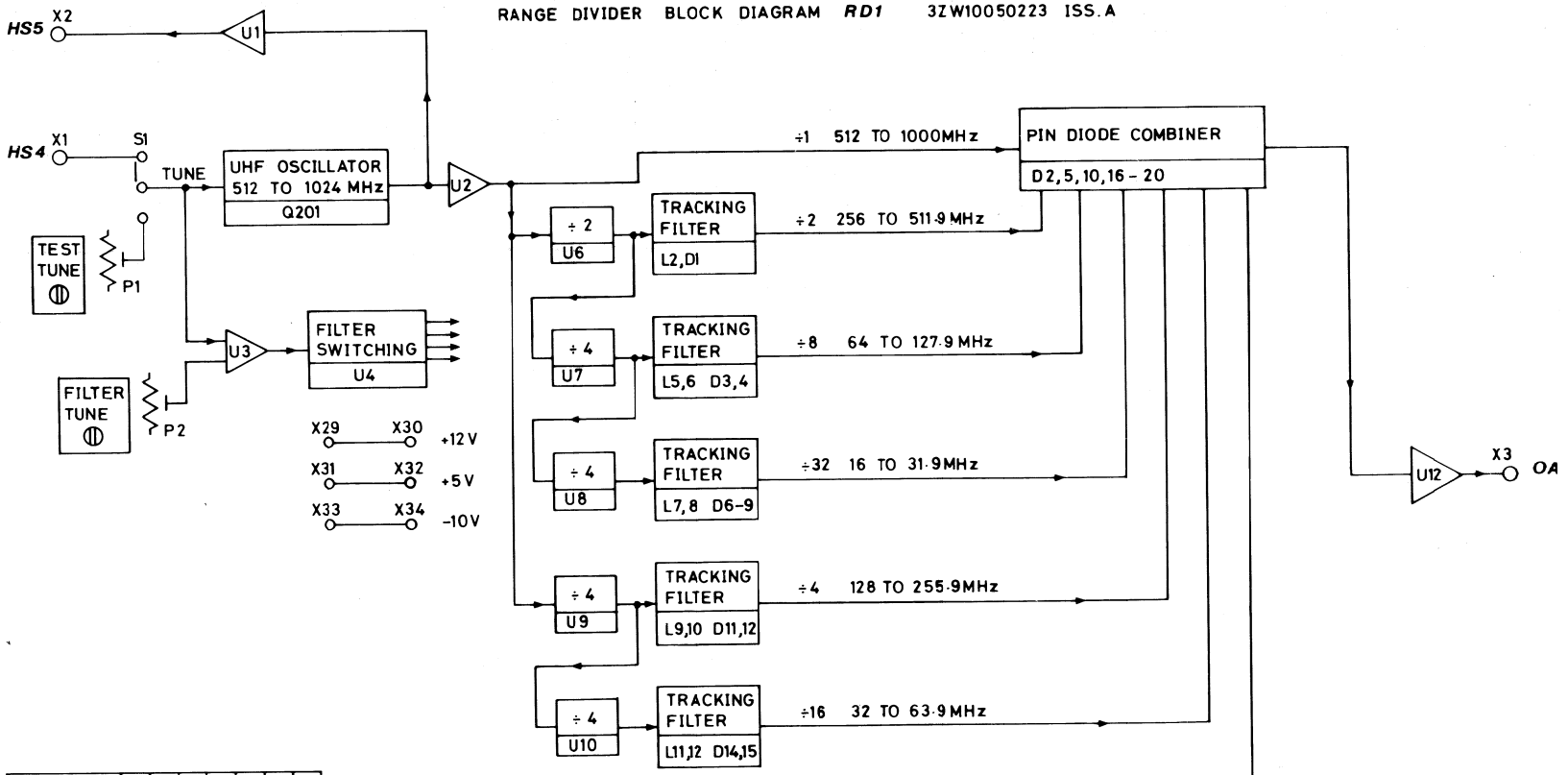
DRAWING NO.
RSZX0322

SHEET OF SHEETS

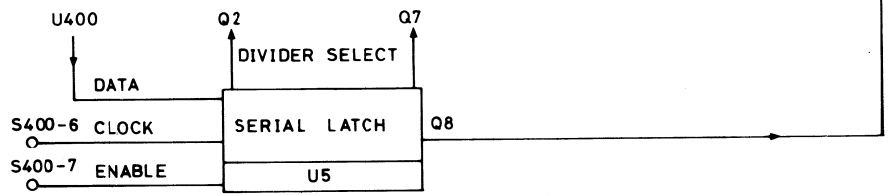
SYNTHESIZER COMPONENT LOCATION

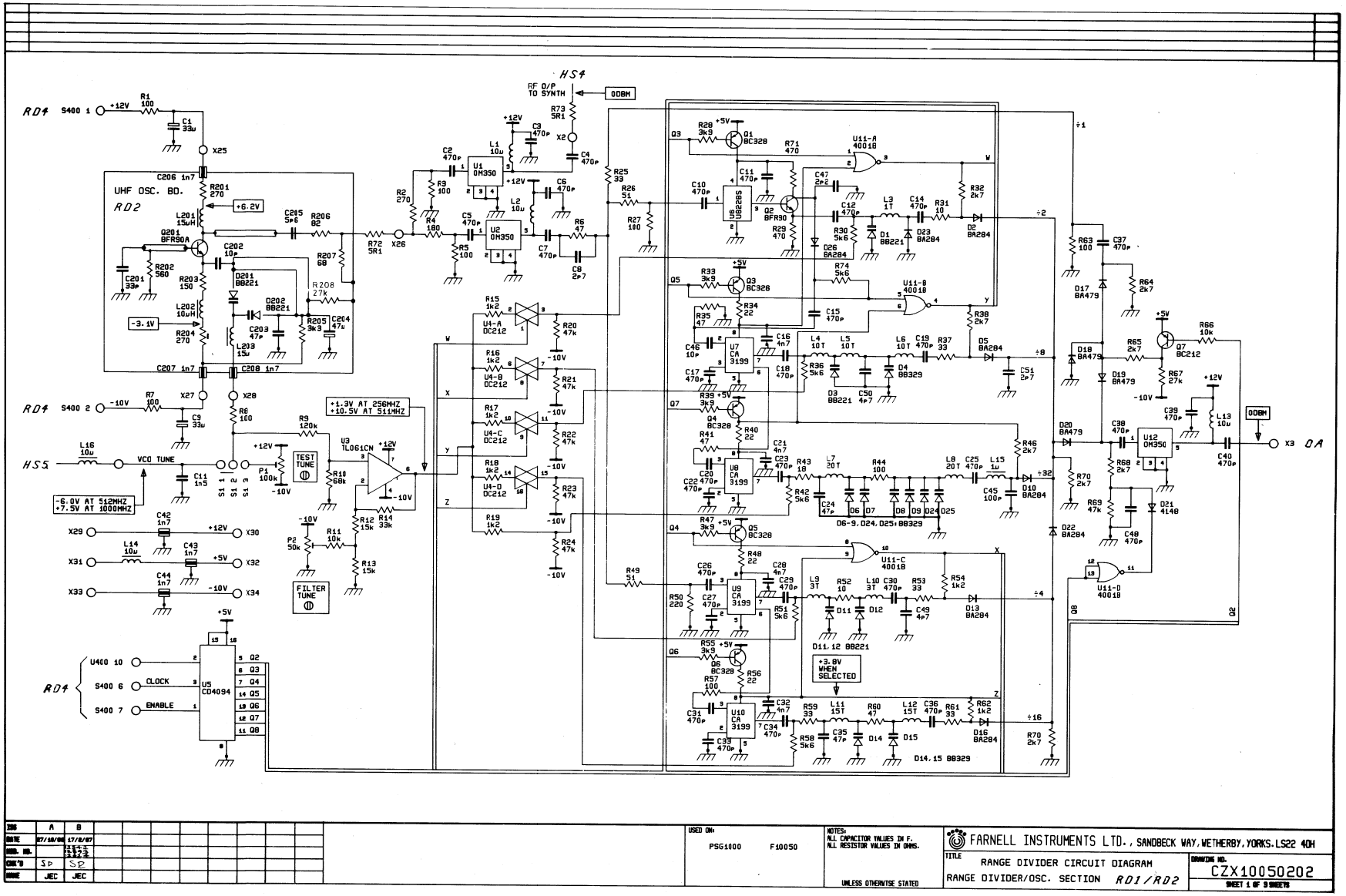


RANGE DIVIDER BLOCK DIAGRAM *RD1* 3ZW10050223 ISS.A



DIVIDER SELECT	Q2	Q3	Q4	Q5	Q6	Q7	Q8
÷ 1	L	H	H	H	H	H	
÷ 2	H	L	H	H	H	H	
÷ 4	H	H	L	H	H	H	
÷ 8	H	L	H	L	H	H	
÷ 16	H	H	L	H	L	H	
÷ 32	H	L	H	L	H	L	
AGC RANGE							
NORMAL							H
EXTENDED							L





ISS	A	B
DATE	07/10/86	17/8/87
MOD. NO.		15573 15573 01222
CHK'D	SP	SP
DRWN	JEC	JEC

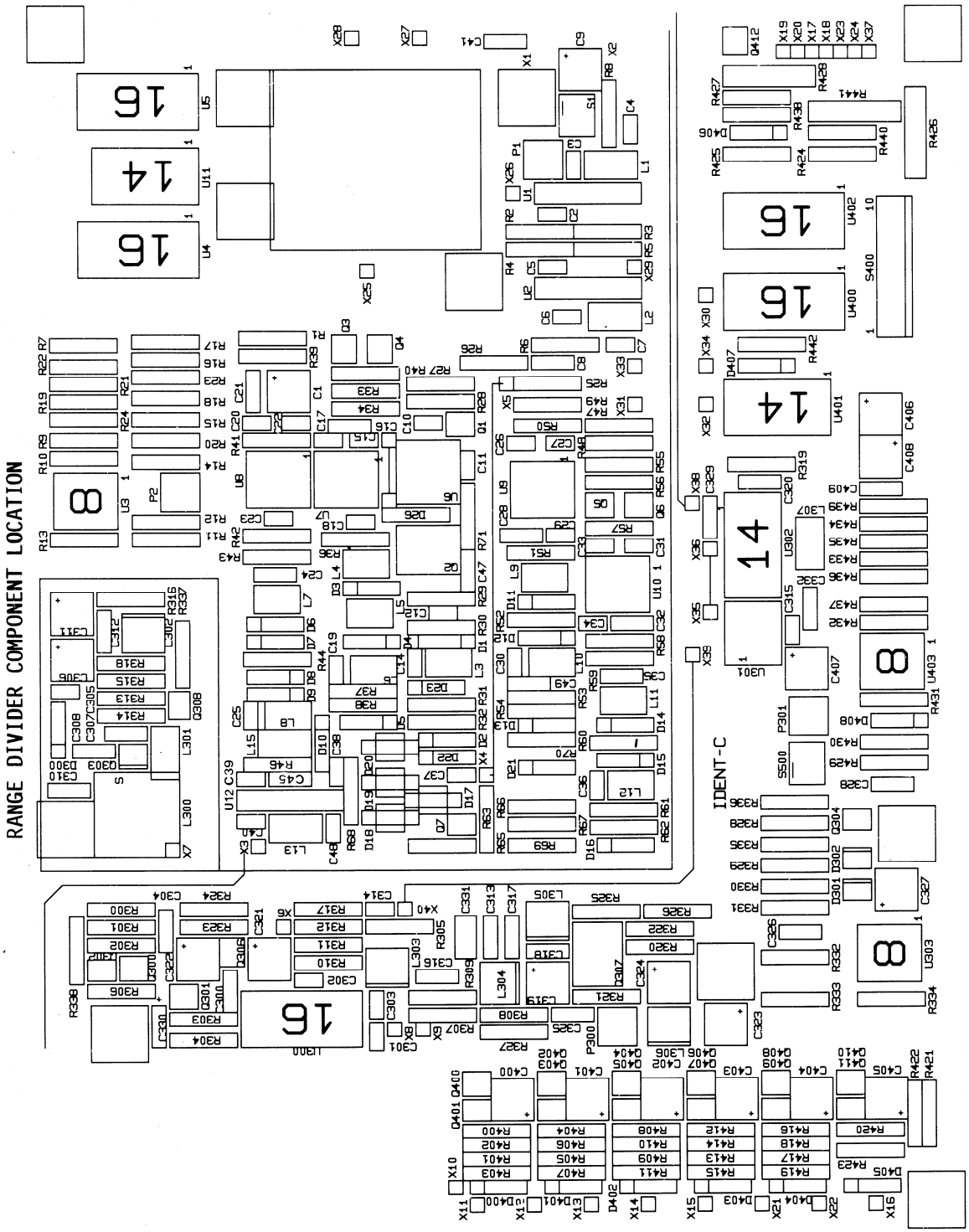
USED ON:
PSG1000 F10050

NOTES:
ALL CAPACITOR VALUES IN F.
ALL RESISTOR VALUES IN OHMS.
UNLESS OTHERWISE STATED

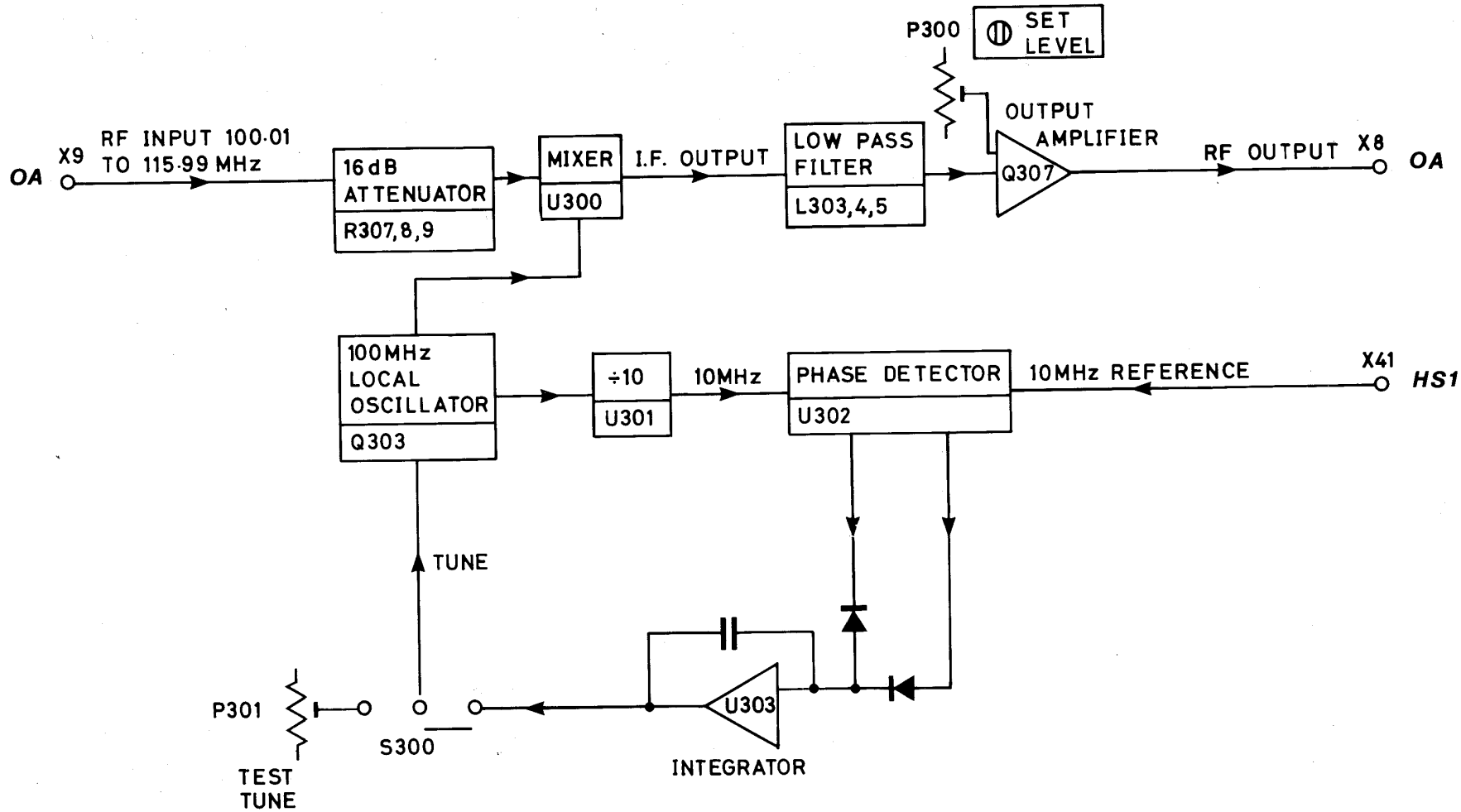
FARNELL INSTRUMENTS LTD., SANDBECK WAY, WETHERBY, YORKS. LS22 4DH

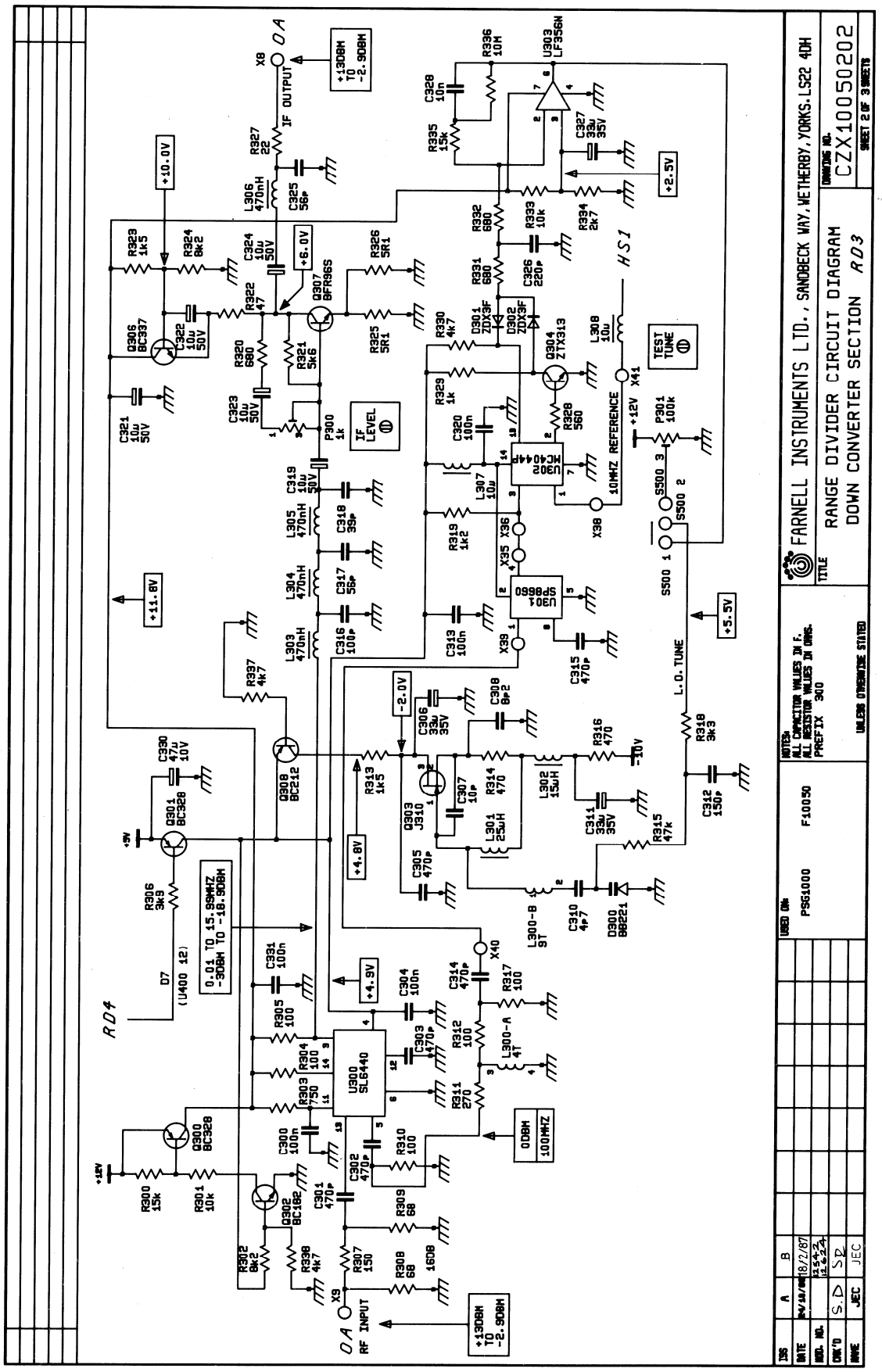
TITLE
RANGE DIVIDER CIRCUIT DIAGRAM
RANGE DIVIDER/OSC. SECTION RD1/RD2

DRAWING NO.
CZX10050202
SHEET 1 OF 3 SHEETS

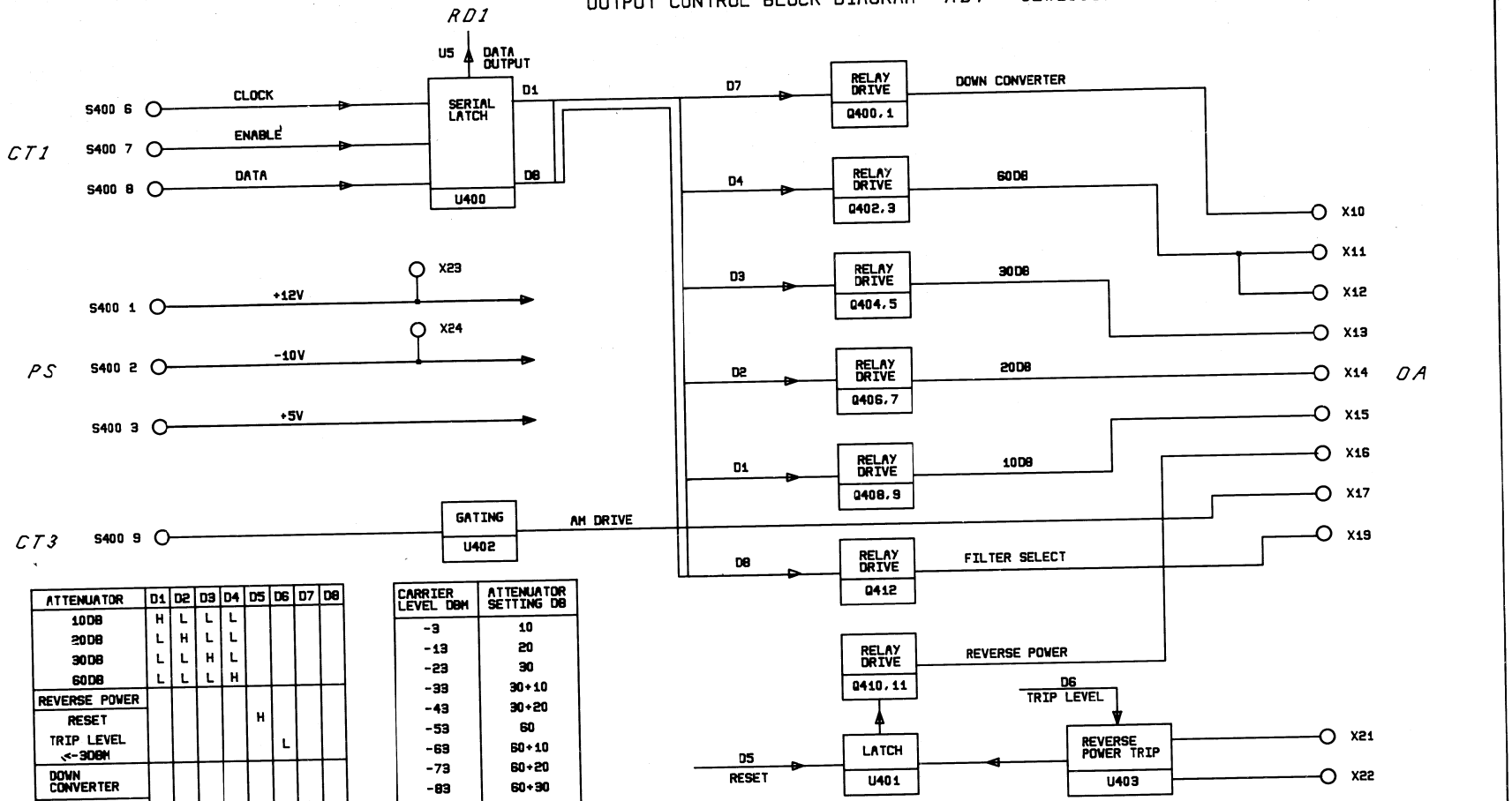

RANGE DIVIDER COMPONENT LOCATION
IDENT-C

DOWN CONVERTER BLOCK DIAGRAM *RD3* 4ZW10050224 ISS. A



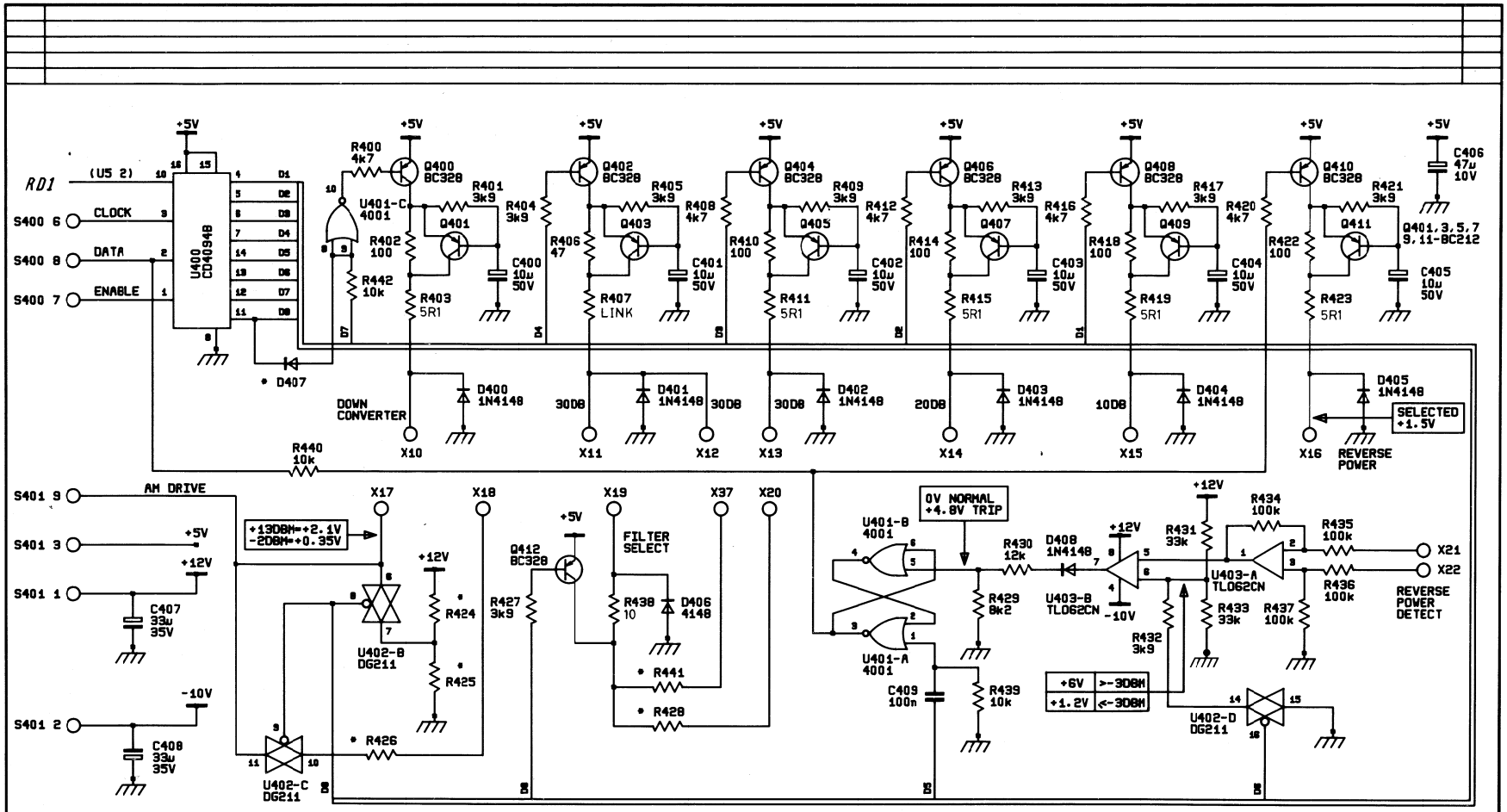

FARNELL INSTRUMENTS LTD., SANDBECK WAY, WETHERBY, YORKS. LS22 4DH
RANGE DIVIDER CIRCUIT DIAGRAM
DOWN CONVERTER SECTION RD3
DRAWING NO. CZX10050202
SHEET 2 OF 3 SHEETS
NOTES: ALL CAPACITOR VALUES IN F. ALL RESISTOR VALUES IN OHMS. PREFIX 900
UNLESS OTHERWISE STATED
USED ON: PSG1000
F10050
RD4
RD3
HS1
IF OUTPUT
RF INPUT
IF LEVEL
TEST TUNE
10MHZ REFERENCE
L.O. TUNE
+13DBM TO -2.9DBM
0.01 TO 15.99MHZ -30DBM TO -16.9DBM
0DBM 100MHZ
U300 SL6440
U303 LF356N
U304 SP8660
U305 TC4424
Q300 BC328
Q301 BC328
Q302 BC182
Q303 J310
Q304 ZTX313
Q306 BC337
Q307 BFR96S
Q308 BC212
D300 BB221
D301 ZDX3F
D302 ZDX3F
+10.0V
+6.0V
+11.8V
+5V
+12V
-2.0V
+4.8V
+4.9V
+2.5V
+5.5V
-10V
X8
X9
X40
X41
X36
X35
X39
S500

OUTPUT CONTROL BLOCK DIAGRAM *RD4* CZW10050225 ISSUE A



ATTENUATOR	D1	D2	D3	D4	D5	D6	D7	D8
10D8	H	L	L	L				
20D8	L	H	L	L				
30D8	L	L	H	L				
60D8	L	L	L	H				
REVERSE POWER RESET TRIP LEVEL <=-30DBM					H	L		
DOWN CONVERTER <=16MHZ							L	
FILTER >16MHZ <64MHZ								H

CARRIER LEVEL DBM	ATTENUATOR SETTING DB
-3	10
-13	20
-23	30
-33	30+10
-43	30+20
-53	60
-63	60+10
-73	60+20
-83	60+30
-93	60+30+10
-103	60+30+20
-113	60+30+20+10
-123	60+30+20+10
|	EXTENDED AGC RANGE
-139	



ISS	A	B
DATE	29/10/86	18/2/87
MOD. NO.		12624
CHK'D	SD	SD
NAME	JEC	JEC

USED ON: PSG1000 F10050

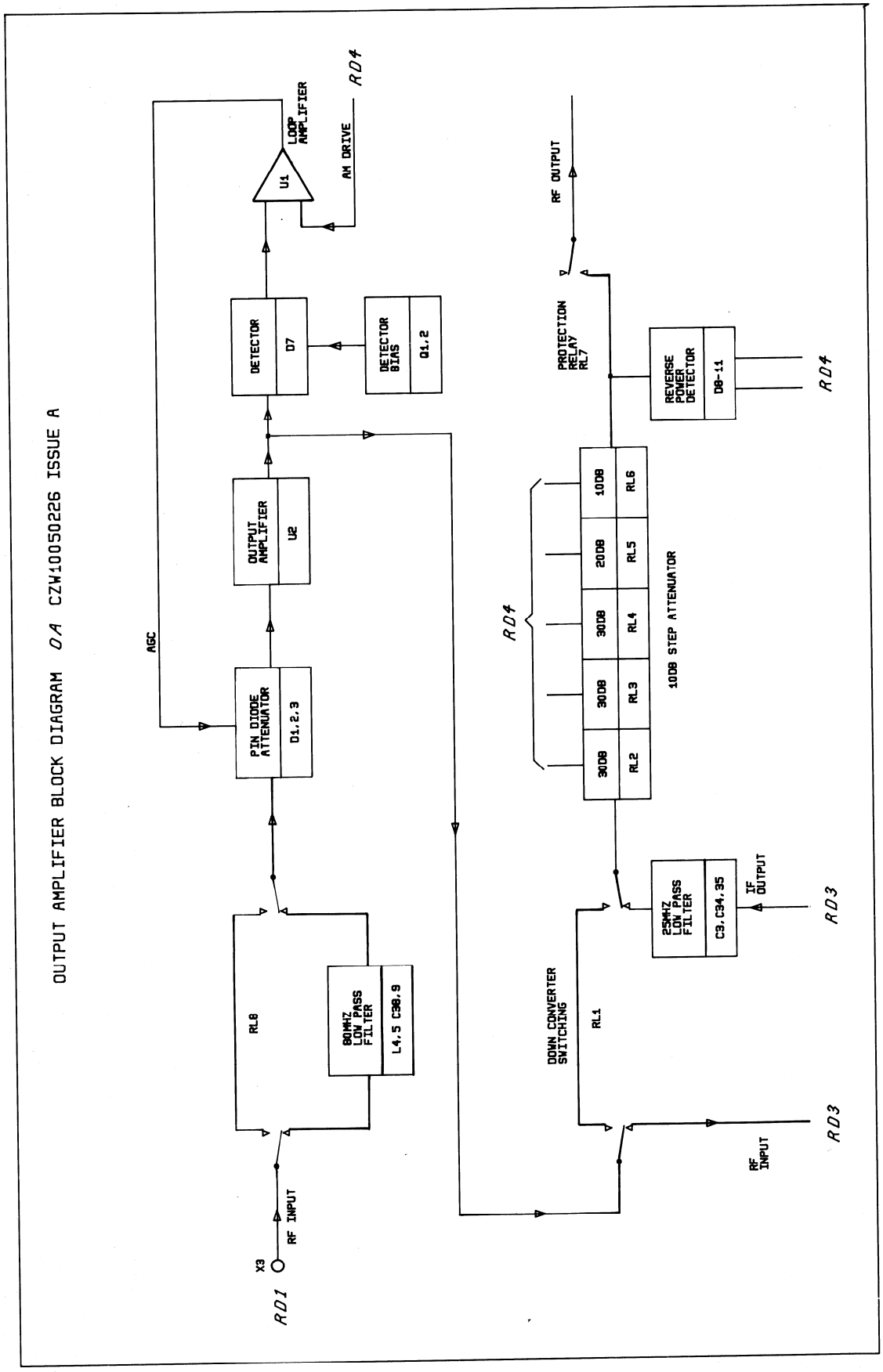
NOTES: ALL CAPACITOR VALUES IN F. ALL RESISTOR VALUES IN OHMS.
* COMPONENT NOT FITTED
UNLESS OTHERWISE STATED

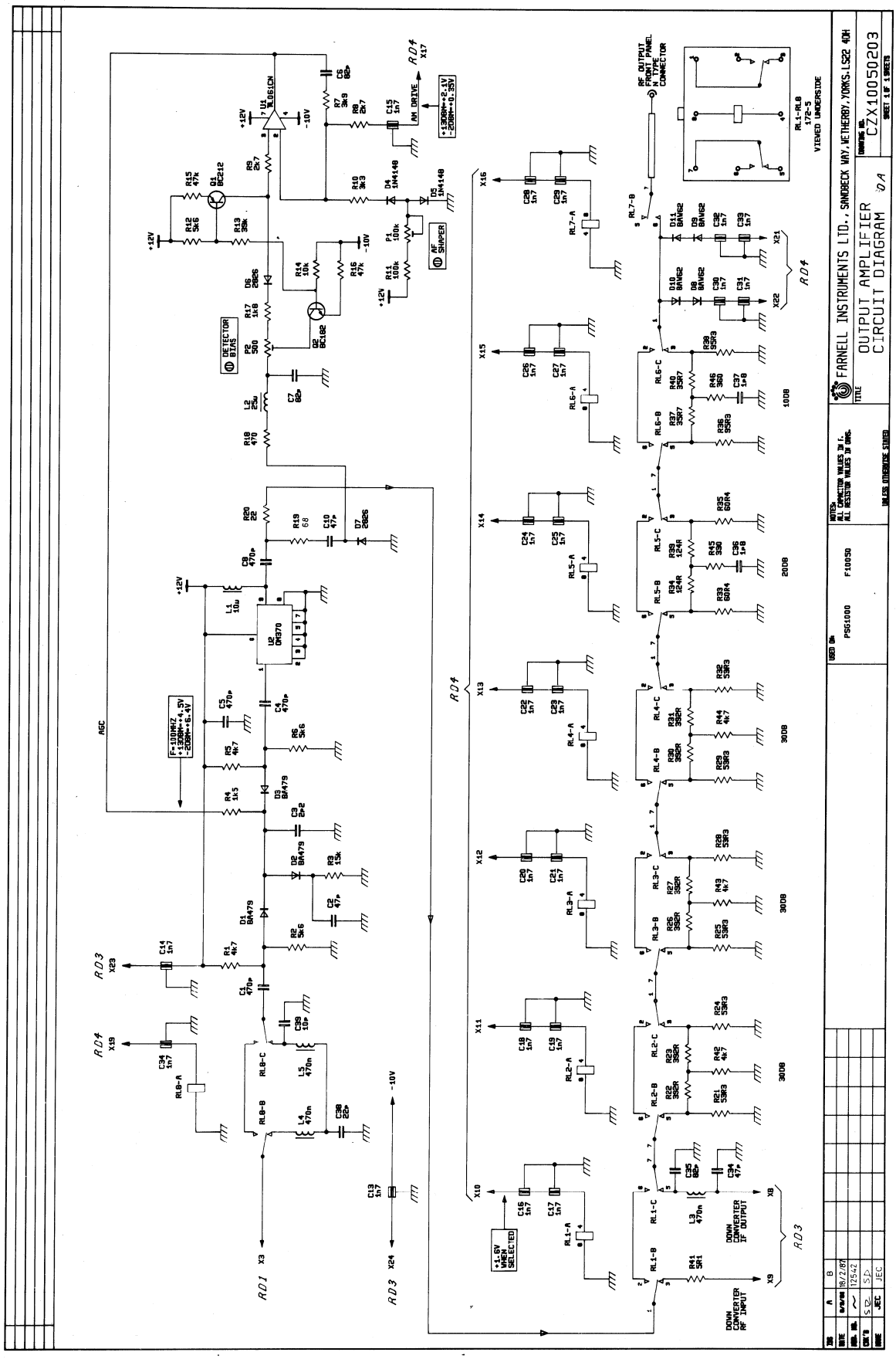
FARNELL INSTRUMENTS LTD., SANDBECK WAY, WETHERBY, YORKS. LS22 4DH

TITLE: RANGE DIVIDER CIRCUIT DIAGRAM
OUTPUT CONTROL SECTION RD4

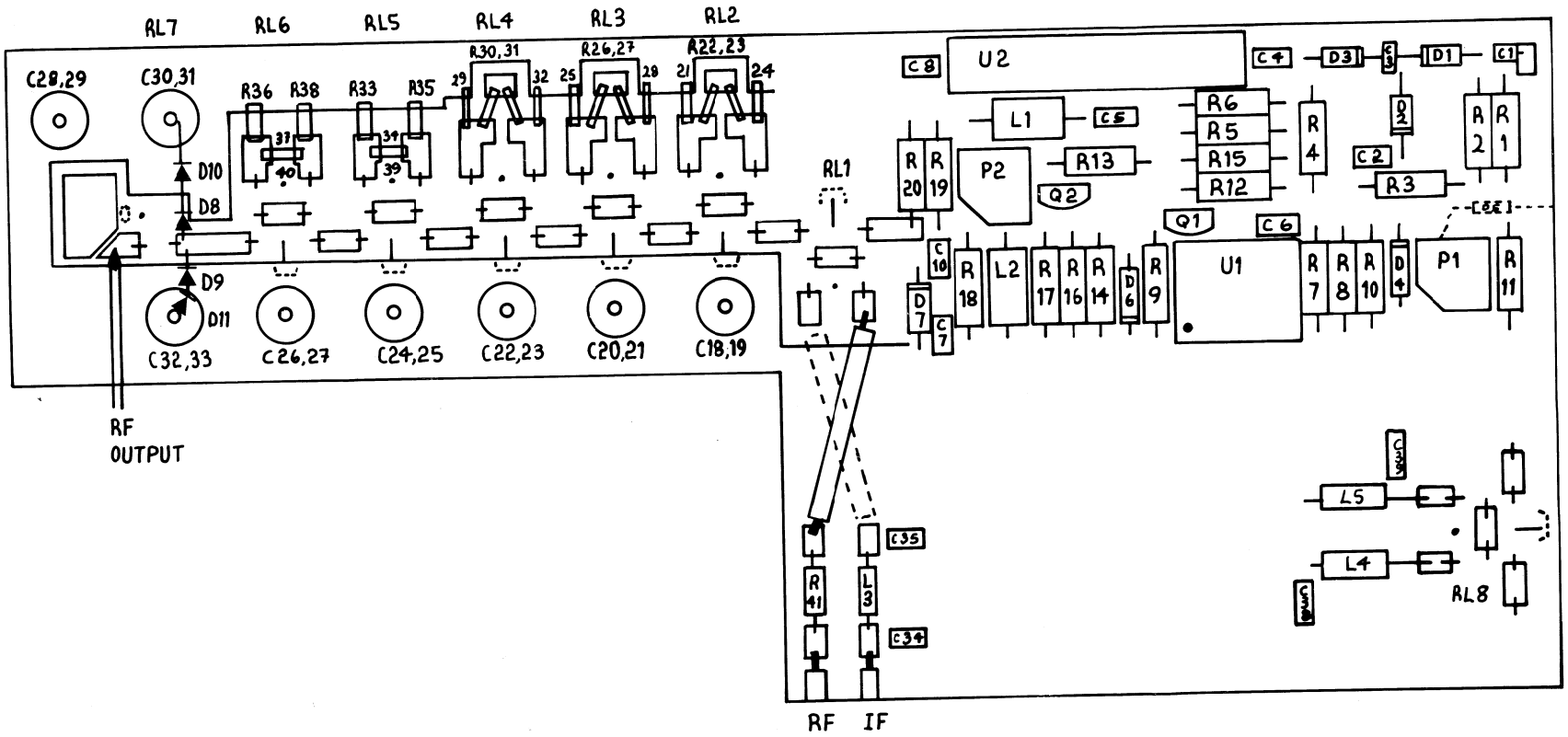
DRAWING NO. CZX10050202

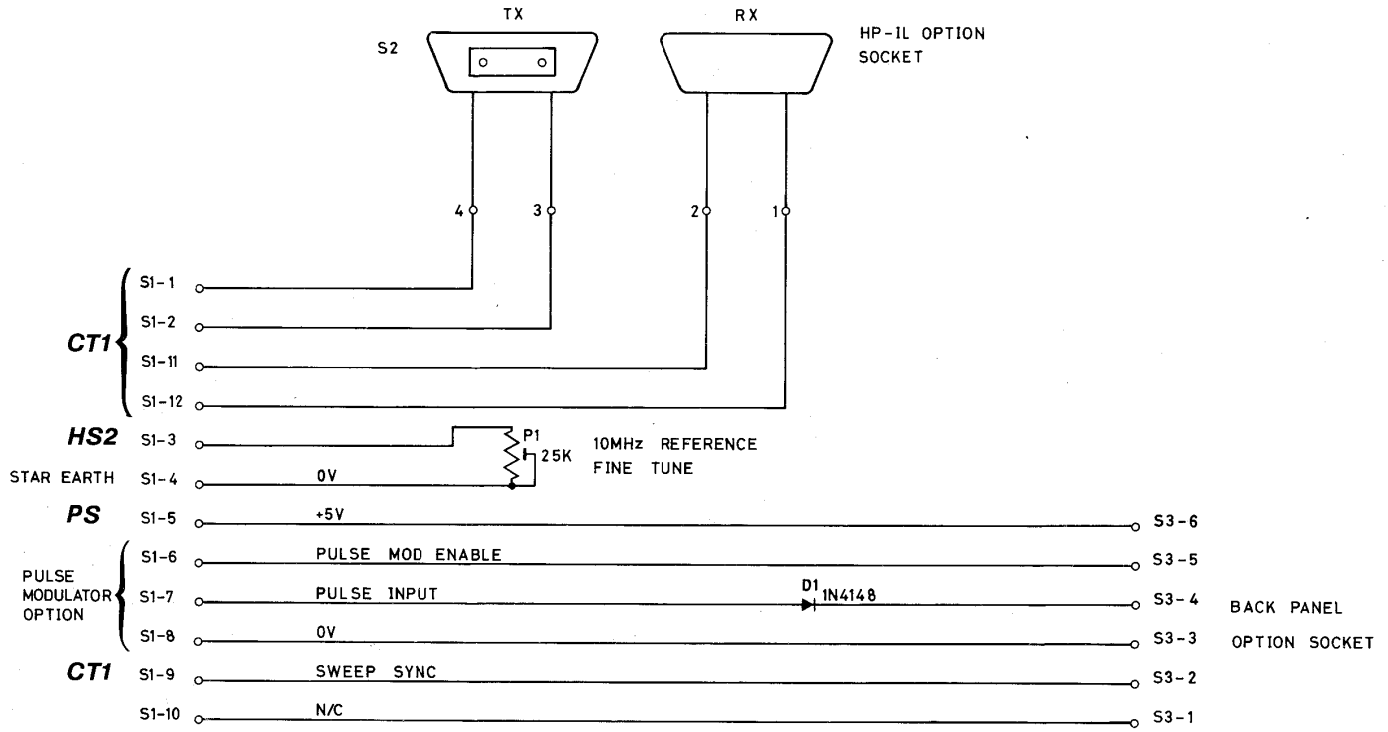
SHEET 3 OF 3 SHEETS


OUTPUT AMPLIFIER BLOCK DIAGRAM 0A CZW10050226 ISSUE A
RD4
LOOP AMPLIFIER
U1
AM DRIVE
DETECTOR
D7
DETECTOR BIAS
Q1.2
OUTPUT AMPLIFIER
U2
AGC
PIN DIODE ATTENUATOR
D1.2.3
RL8
80MHZ LOW PASS FILTER
L4.5 C30.9
X3
RF INPUT
RD1
RF OUTPUT
PROTECTION RELAY RL7
REVERSE POWER DETECTOR
D8-11
RD4
RD4
10DB
20DB
30DB
30DB
30DB
RL6
RL5
RL4
RL3
RL2
10DB STEP ATTENUATOR
DOWN CONVERTER SWITCHING
RL1
25MHZ LOW PASS FILTER
C3, C34, 35
IF OUTPUT
RD3
RF INPUT
RD3


FARNELL INSTRUMENTS LTD., SANDBECK WAY, WETHERBY, YORKS. LS22 4DH
OUTPUT AMPLIFIER
CIRCUIT DIAGRAM
CZX10050203
SHEET 1 OF 1 SHEETS
PSG1000
F10050
DOWN CONVERTER RF INPUT
DOWN CONVERTER IF OUTPUT
RF OUTPUT FRONT PANEL N TYPE CONNECTOR
AGC
AM DRIVE
AF SHAPER
DETECTOR BIAS
+1.6V WHEN SELECTED

37DKK10383 PSG1000 OUTPUT AMPLIFIER/ATTENUATOR COMPONENT IDENT





TRACED	ISS.	DATE	MOD. No.	ISS.	DATE	MOD. No.	USED ON:
1							
CHECKED SP							
DRAWN	A	11.2.87	—				

NOTE:
CAPACITOR VALUES GIVEN IN μF.
RESISTOR VALUES IN Ω
UNLESS OTHERWISE STATED.

FARNELL INSTRUMENTS LTD. WETHERBY, YORKS.

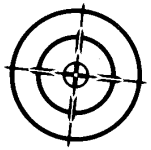
TITLE AUXILIARY CIRCUIT BOARD **AX**

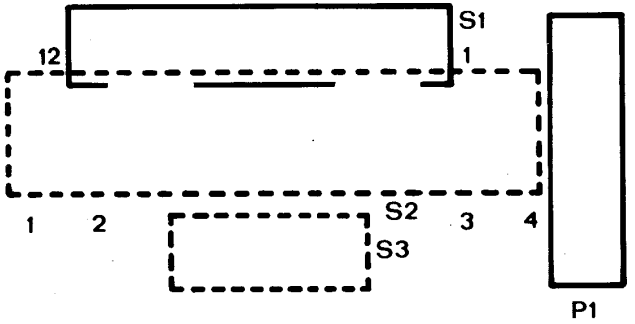
DRAWING No. 3ZX10050207

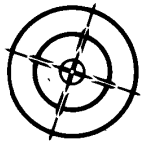
SHEET 1 OF SHEETS

AARQUE 9256/84

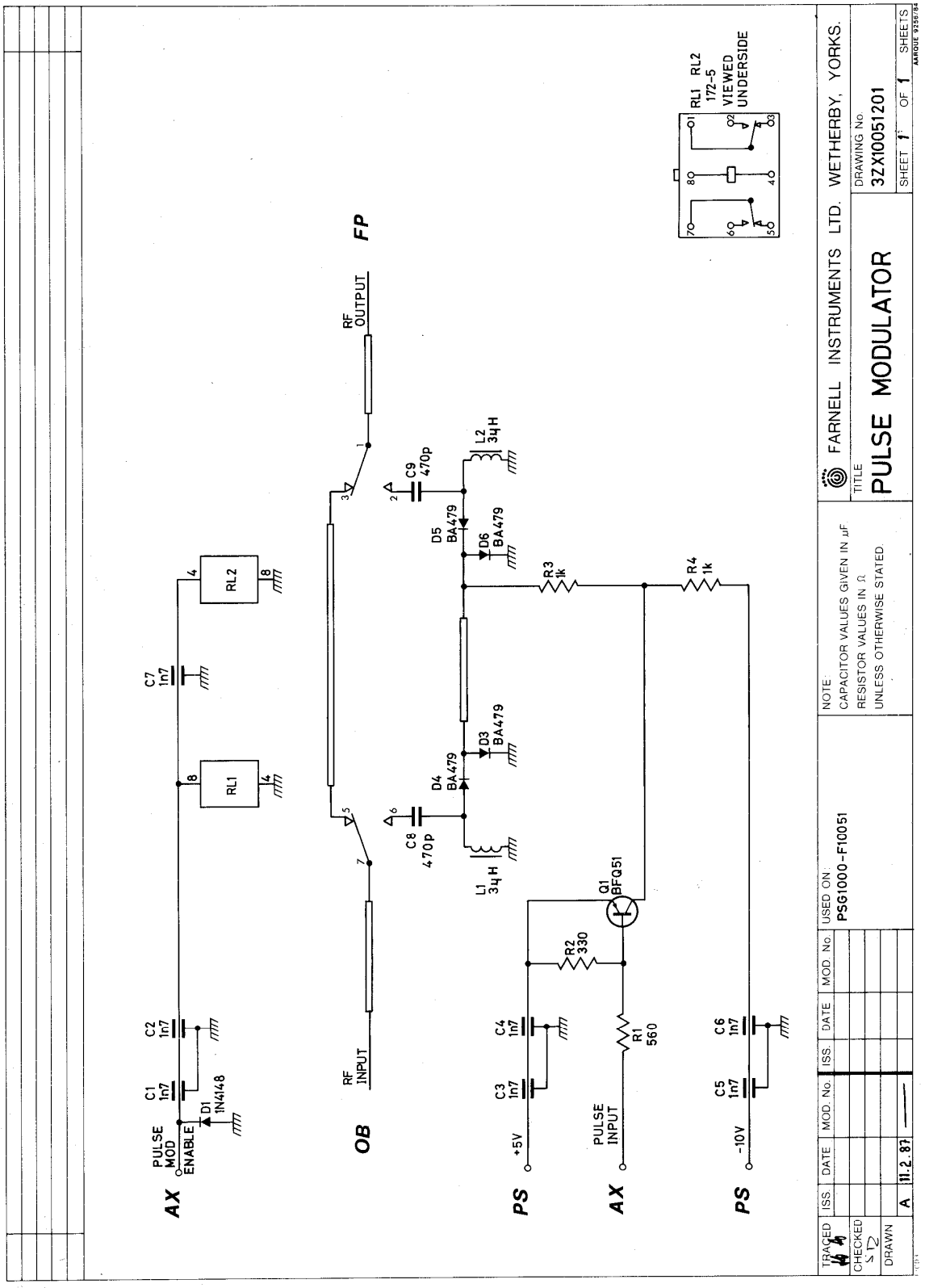
AUXILIARY COMPONENT LOCATION







IDENT-A


PULSE MOD ENABLE
AX
C1 1n7
C2 1n7
D1 1N4148
RL1
RL2
C7 1n7
OB
RF INPUT
RF OUTPUT
FP
C8 470p
C9 470p
L1 3μH
L2 3μH
D4 BA479
D3 BA479
D5 BA479
D6 BA479
R3 1k
R4 1k
Q1 BFQ51
R2 330
R1 560
C4 1n7
C3 1n7
+5V
PS
PULSE INPUT
AX
C6 1n7
C5 1n7
-10V
PS
RL1 RL2 172-5 VIEWED UNDERSIDE
TRACED
CHECKED
DRAWN
ISS.
DATE
MOD. No.
A 11.2.87
USED ON: PSG1000-F10051
NOTE: CAPACITOR VALUES GIVEN IN μF RESISTOR VALUES IN Ω UNLESS OTHERWISE STATED
FARNELL INSTRUMENTS LTD. WETHERBY, YORKS.
TITLE
PULSE MODULATOR
DRAWING No.
3ZX10051201
SHEET 1 OF 1 SHEETS

12. CONNECTION LISTS

12.1 POWER SUPPLY (PS)

CONNECTOR	TITLE	DESTINATION
S1 - 1	+5V Secondary	TX1
2	+5V Secondary	TX1
3	0V	TX1
4	+12V Secondary	TX1
5	+12V Secondary	TX1
6	-10V Secondary	TX1
7	-10V Secondary	TX1
8	-	-
9	-	-
10	Relay Coil	RL1
11	Inverter	TX1
12	Inverter	RL1
13	Battery -ve	S4
14	Inverter	RL1
15	Battery +ve	S4
S2 - 1	+5V	RD4 S400-3
2	+5V	HS2 S201-5
3	0V	Star Earth
4	0V	Star Earth
5	+5V	DP S3-1
6	+5V	CT1 S103-12
S3 - 1	Battery Level	CT1 S103-6
2	0V	Star Earth
3	-10V	RD4 S400-2
4	-10V	HS2 S201-4
5	-10V	CT3 S302-7
6	Secondary Sense	CT1 S103-11
7	+12V	RD4 S400-1
8	+12V	HS2 S201-3
9	+12V	CT3 S302-9
10	0V	Star Earth

12.2 CONTROL (CT1, 2, 3, 4)

CONNECTOR	TITLE	DESTINATION
S101	20 Way Ribbon Cable	DP S2
S102	24 Way Ribbon Cable	Back Panel IEEE Socket
S103-1	-	-
2	-	-
3	-	-
4	-	-
5	Sweep Sync	Back Panel
6	Battery State	PS S3-1
7	HP-IL RX	Back Panel
8	HP-IL RX	Back Panel
9	HP-IL TX	Back Panel
10	HP-IL TX	Back Panel
11	Secondary Sense	PS S3-6
12	+5V	PS S2-6
S301-1	-	-
2	Meter Drive	DP S4-2
3	+12V	DP S4-3
4	Screen	DP S4-4
5	Level Pot Wiper	DP S4-5
6	Screen	DP S4-6
7	Level Pot	DP S4-7
8	Modulation Input/Output	DP S4-8
9	Screen	DT S4-9
10	SINAD Input	DP S4-10
11	Screen	DP S4-11
12	Click Relay	DP S4-12
S302-1	-	-
2	Output Enable EN2	RD4 S400-7
3	Output Clock	RD4 S400-6
4	Output Data	RD4 S401-8
5	Screen	OB
6	AM Drive	RD4 S400-9
7	-10V	PS S3-5
8	OV	Star Earth
9	+12V	PS S3-9
10	-	-
11	Synthesizer Clock	HS2 S201-6
12	Synthesizer Data	HS2 S201-7
13	Synthesizer Enable EN1	HS2 S201-10
14	Synthesizer Enable EN0	HS2 S201-8
15	FM Drive	HS2 S201-9
16	Screen	SB

12.3 DISPLAY (DP)

CONNECTOR	TITLE	DESTINATION
S1	14 Way Ribbon Cable	Membrane Front Panel
S2	20 Way Ribbon Cable	CT1 S101
S3-1	+5V	PS S2-5
2	OV	Star Earth
S4-1	-	-
2	Meter Drive	CT4 S301-2
3	+12V	CT3 S301-3
4	Screen	CT3 S301-4
5	Level Pot Wiper	CT3 S301-5
6	Screen	CT3 S301-6
7	Level Pot	CT3 S301-7
8	Modulation Input/Output	CT3 S301-8
9	Screen	CT3 S301-9
10	SINAD Input	CT4 S301-10
11	Screen	CT4 S301-11
12	Click Relay	CT1 S301-12
X1	Meter Drive	Front Panel Meter
X2	OV	Front Panel Meter
X3	Modulation Input/Output	Front Panel BNC

12.4 SYNTHESIZER(HS1-7)

CONNECTOR	TITLE	DESTINATION
S201-1	10MHz Fine Tune	Back Panel
2	-	-
3	+12V	PS S3-8
4	-10V	PS S3-4
5	+5V	PS S2-2
6	Synthesizer Clock	CT1 S302-11
7	Synthesizer Data	CT1 S302-12
8	Synthesizer Enable EN0	CT1 S302-14
9	FM Drive	CT3 S302-15
10	Synthesizer Enable EN1	CT1 S302-13
X103	10MHz Reference	RD3 X41
X104	10MHz Reference Input/Output	Back Panel BNC
X405	UHF Oscillator Tune	RD1 X1
X505	UHF Signal	RD1 X2

12.5 RANGE DIVIDER (RD1, 2, 3, 4)

CONNECTOR	TITLE	DESTINATION
S400-1	+12V	PS S3-7
2	-10V	PS S3-3
3	+5V	PS S2-1
4	-	-
5	-	-
6	Output Clock	CT1 S302-3
7	Output Enable EN2	CT1 S302-2
8	Output Data	CT1 S302-4
9	AM Drive	CT3 S302-6
10	-	-
X1	Tuning Input	HS5 X505
X2	UHF Signal	HS4 X405
X41	10MHz Reference	HS1 X103
X3	RF Input	OA
X8	Down Converter RF Output	OA
X9	Down Converter RF Input	OA
X10	Down Converter Select	OA
X11	30dB Select	OA
X12	30dB Select	OA
X13	30dB Select	OA
X14	20dB Select	OA
X15	10dB Select	OA
X16	Reverse Power Select	OA
X17	AM Drive	OA
X19	Filter Select	OA
X21	Reverse Power Detect -ve	OA
X22	Reverse Power Detect +ve	OA
X23	+12V	OA
X24	-10V	OA

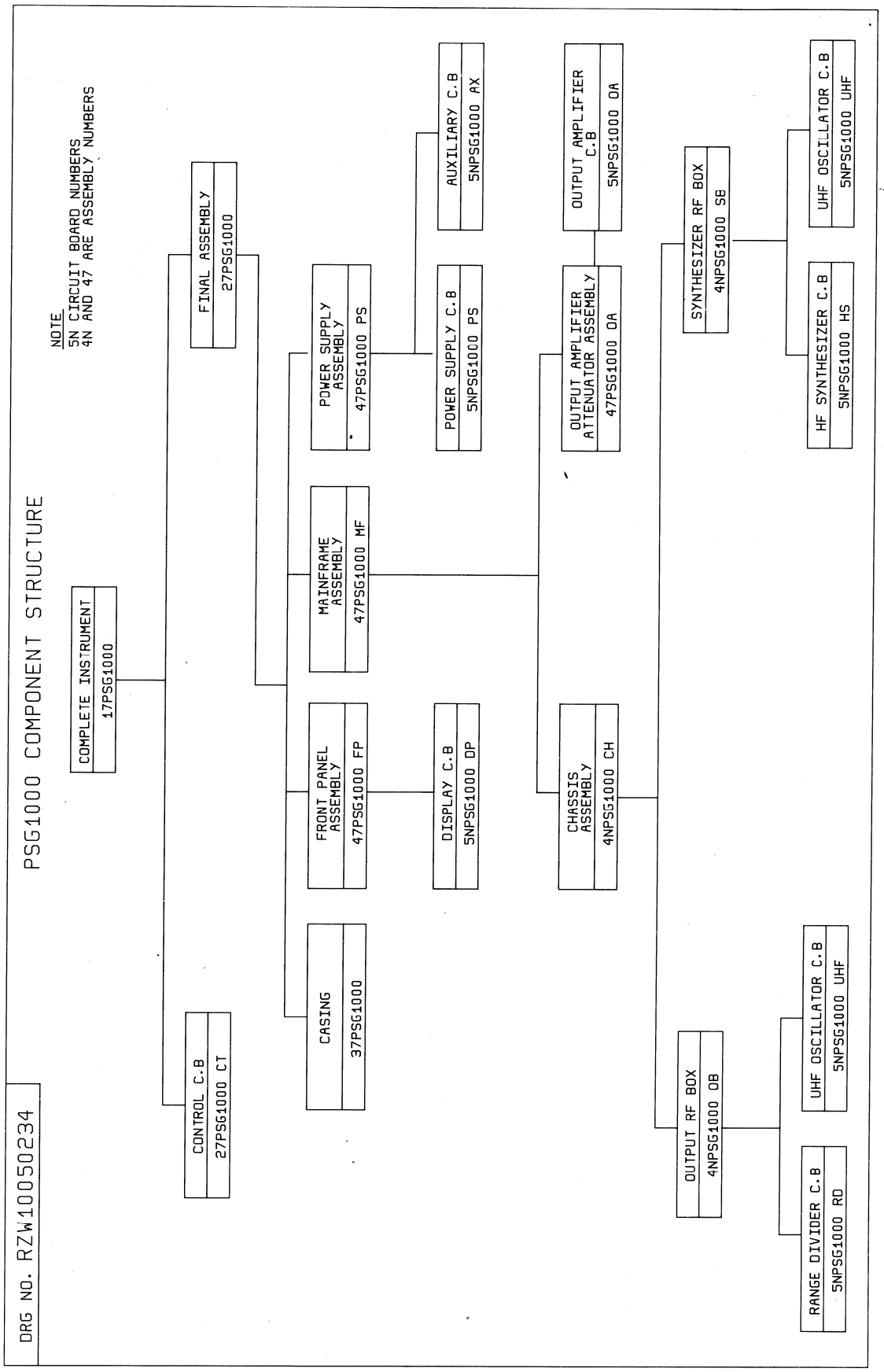
12.6 AUXILIARY CIRCUIT BOARD (AX) (LOCATED ON BACK PANEL)

CONNECTOR	TITLE	DESTINATION
S1-1	HP-IL TX	CT1 S103-9
2	HP-IL TX	CT1 S103-10
3	10MHz Fine tine	HS2 S201-1
4	0V	Star earth
5	+5V	Power supply
6	Pulse mod enable	Pulse modulator - option
7	Pulse input	Pulse modulator - option
8	0V	Pulse modulator - option
9	Sweep sync	CT1 S103-5
10	-	-
11	HP-IL RX	CT1 S103-7
12	HP-IL RX	CT1 S103-8

BACK PANEL AUXILIARY CONNECTIONS

S3-1	+5V	link to enable	only present for pulse modulator option
2	Pulse mod enable		
3	Pulse input		
4	0V		
5	Sweep sync		
6	-		-

13. COMPONENTS LIST



MAIN UNIT ITEM NUMBER : 17PSG1000 DESCRIPTION : TEL/N *PSG1000 *0050

IMPORTANT EXPLANATION - PLEASE READ BEFORE ORDERING PARTS.
DUE TO LIMITATIONS IN THE NUMBER OF CHARACTER SPACES AVAILABLE THE INFORMATION IN THE CIRCUIT REFERENCE FIELD HAS BEEN ABBREVIATED AND THE FOLLOWING NOTES ARE PROVIDED AS A GUIDE TO IT'S INTERPRETATION:

1. WHERE A COMPONENT IS USED MORE THAN ONCE ON AN ASSEMBLY THE ALPHABETIC PORTION OF THE CIRCUIT REFERENCE FOR ITS SECOND AND SUBSEQUENT LOCATIONS HAS BEEN OMITTED; EG. THE CIRCUIT REFERENCE INFORMATION FOR A COMPONENT LOCATED AT R1 AND R6 WILL APPEAR AS R1 6
2. THE CIRCUIT REFERENCE NUMBERS ARE PRESENTED IN ASCENDING DECADE BLOCKS DELIMITED BY COLONS: SECOND AND SUBSEQUENT NUMBERS WITHIN A DECADE BLOCK REPRESENT ONLY THE UNIT VALUE OF THE LOCATION (THE TENS AND HUNDREDS VALUES BEING IMPLIED); EG. FOR A COMPONENT LOCATED AT R54,R57,R59,R82,R87,R102,R110, AND R112 THE CIRCUIT REFERENCE ENTRY WILL BE R54 7 9:82 7:102:10 2
3. WHERE COMPONENTS ARE USED IN A SERIES OF NEIGHBOURING CIRCUIT REFERENCE LOCATIONS THE CIRCUIT REFERENCE NUMBERS ARE REPRESENTED AS INCLUSIVE BLOCKS USING A HYPHEN; EG. A COMPONENT LOCATED AT R16,R19,R21,R24,R25,R26,R31,R37,R38,R39,R40,R44 AND R46 WILL BE REPRESENTED AS R16 9:21 4-6:31 37-40 4 6 (AN EXCEPTION TO THE RULES OCCURS WHEN A SERIES CROSSES A DECADE BLOCK IN WHICH CASE THE TENS VALUE IS INSERTED.
4. COMMENTS ARE PRECEDED BY A SEMICOLON.

WHEN ORDERING REPLACEMENT PARTS PLEASE BE SURE TO QUOTE THE PART NUMBER PROVIDED.

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE	
27PSG1000		END ITEM:	FIN/B *FINAL ASM
37PSG1000		CASING:	CAS/B *PSG1000
TG212	PLUG 3 POLE RPC212RB3P	PL4	
47PSG1000FP		ASSEMBLY:	FIN/C *F/PANEL
5NPSG1000DP		CCT BOARD:	CPS/C *DISPLAY CB
CC44K70N630	4K7PF 100V 630-19472	C1-4	
CD41K751214	F/CAP 1K75PF ERI 1214	C6	
CE233U0IEK	33UF 35V KMVB ECC	C5	
DG4148	DIODE 1N4148 REEL	D1	
PM550K063X	50KR SPL 63X	P2	
VA5450N	IC MM5450N *STATIC	U1-4	
SRG2V5	G2E 5V ORM	RL1	
TIH2520NR1S	20W M52-1220-450 PYE	S2	
TBM2512PT	12W 4094 22 05 2125	S4	
LD5551	LED RED HDSP5551 GD"B"	LED1-12	
LD1301RED	LED HLMP-1301 RED	LED13-39	
TBM3902PR	2W 2420-09-75-1021	S3	
TBM2506P0	SKT 6W 4030-22-03-2061	X5	
TBM2514PT	SKT 14W 4094-22-05-214	S1	
PM6100K12P	100KR LIN 12PE	P1	
BC1041	C /D *DISPLAY *7RBT	B	
RW13R3021	3R3 5% WEL W21/74ER	R5	
TP1510	CB PIN MR15100 TUC	X1-X4	
VS40L	IC SKT 703-1340-010410	U1-4	
EM0017	3SM/B *PSG1000	M1	
RM580K6251	80K6 1% MUL MRS25	R1-4	
TR10942	N B/HEAD UT085 SK1094/	S3	
TR004N	SKT LX04-0503-ZZ004N	S1 2	
47PSG1000MF		ASSEMBLY:	FIN/A *MAIN FRAME ASM

MAIN UNIT ITEM NUMBER : 17PSG1000 DESCRIPTION : TEL/N *PSG1000 *0050

FARNELL PART NUMBER	DESCRIPTION	*---------- CIRCUIT REFERENCE ----------*
4NPSG1000CH		ASSEMBLY: SUB/E *CHASSIS ASSY
4NPSG10000B		ASSEMBLY: SUB/A *OUTPUT BOX
5NPSG1000RD		CCT BOARD: CPS/H *RANGE DIVIDER
5NPSG1000RD3		CCT BOARD: CPS/F *DOWN CONVERTER
RM15R1025	5R1 1% MRS25 REEL	R325 6
RM222R025	22R 1% MUL MRS25	R327
RM247R025	47R 1% MRS25 REEL	R322
RM268R025	68R 1% MUL MRS25	R308 9
RM3100R25	100R 1% MRS25 REEL	R304 5:10-12 7
RM3150R25	150R 1% MUL MRS25	R307
RM3470R25	470R 1% MRS25 REEL	R314 6
RM3560R25	560R 1% MRS25 REEL	R328
RM3680R25	680R 1% MUL MRS25	R320:31 2
RM3750R25	750R 1% MRS25 REEL	R303
RM41K2025	1K2R 1% MRS25 REEL	R319
RM41K5025	1K5R 1% MRS25 REEL	R313:23
RM42K7025	2K7R 1% MRS25 REEL	R334
RM43K3025	3K3R 1% MRS25 REEL	R318
RM43K9025	3K9R 1% MUL MRS25	R306
RM44K7025	4K7R 1% MRS25 REEL	R330 7 8
RM45K6025	5K6R 1% MUL MRS25	R321
RM48K2025	8K2R 1% MRS25 REEL	R302:24
RM510K025	10KR 1% MRS25 REEL	R301:33
RM515K025	15KR 1% MRS25 REEL	R300:35
RM547K025	47KR 1% MRS25 REEL	R315
RC810M025	10MR 10% MUL CR25	R336
CC12P20N642	2P2F 100V 683-09228	C309
CC14P70N642	4P7F 100V 683-09478	C310
CC18P20N642	8P2F 100V 683-09828	C308
CC210P0N642	10PF 100V 683-10109	C307
CC239P0N642	39PF 100V 683-34399	C318
CC256P0N642	56PF 100V 683-34569	C317:25
CC3100PN642	100PF 100V 683-34101	C316
CC3150PN642	150PF 100V 683-34151	C312
CC3220PN683	220PF 100V 683-58221	C326
CC3470PN630	470PF 100V 630-18471	C301-303 5:14 5
CE247U0DFC	47UF 10V KMVB 5 PITCH	C330
CFOU100LMKS	0.1UF 63V WIM MKS2MIN	C300 4:13:20:31 2
CF510K0NFKS2	10KPF 100V 5% WIM FKS2	C328
DG221	DIODE BB221 ITT	D300
DGD3F	DUAL ZDX3F FER	D301 2
VA6440CDP	INT CCT SL6440CDP	U300
VA8660DP	INT CCT SP8660DP	U301
VA356TC	IC UAF356TC/LF356N	U303
VD4044P	INT CCT MC4044P	U302
VT328	BC328 TO-92D	Q300 1
VT182PL	BC182PL E-LINE	Q302
VT337	BC337 TO-92D	Q306
VTX313	ZTX313 E-LINE	Q304
VTR96S	TRANS BFR96S MUL ONLY	Q307
ZC15U10	CHOKE 15UH SC10 ITT	L302
ZC0U510	CHOKE 0U5H SC10 0U47H	L303-306
ZC0292	3SR/A *YE315S 6 TURNS	L301
VF310S	J310 SILICONIX *STATIC	Q303
TBM2503P0	3w 4030 22-03-2031	SK500
RM327R25	27OR 1% MRS25 REEL	R311

MAIN UNIT ITEM NUMBER : 17PSG1000 DESCRIPTION : TEL/N *PSG1000 *0050

FARNELL PART NUMBER	DESCRIPTION		CIRCUIT REFERENCE
RM41K0025	1KOR 1% MRS25	REEL	R329
ZZ9F30131	3 /B *CHK R/DIV PSG		L300
PM41K0067T	1KOR TYPE 67T		P300
ZC0290	3SR/B *YE315S 4 TURNS		L307
VS16L	IC SKT 703-1316-010410		U300
VS14L	IC SKT 703-1314-010410		U302
VS8P	IC SKT 703-1308-010410		U303
VT212PL	BC212PL	E-LINE	Q308
CAOMIT	CAPACITORS OMITTED		C329
PM6100K67T	100K TYPE 67T		P301
CE233U0IFC	33UF 35V KMVBFC 5 PITC		C306:11:27
CE210U0KFC	10UF 50V KMVBFC 5 PITC		C319:21-24
5NPSG1000RD4			CCT BOARD: CPS/C *OUTPUT CONTROL
RM247R025	47R 1% MRS25	REEL	R406
RM3100R25	100R 1% MRS25	REEL	R402:10 4 8:22 8:41
RM43K9025	3K9R 1% MUL MRS25		R401 4 5 9:13 7:21 7:32
RM44K7025	4K7R 1% MRS25	REEL	R400 8:12 6:20
RM48K2025	8K2R 1% MRS25	REEL	R429
RM510K025	10KR 1% MRS25	REEL	R439:40 2
RM512K025	12KR 1% MRS25	REEL	R430
RM533K025	33KR 1% MUL MRS25		R431 3
RM6100K25	100K 1% MRS25	REEL	R434-37
RASOT	**** SELECT ON TEST **		R426
CE247U0DFC	47UF 10V KMVB 5 PITCH		C406
CFOU100LMKS	0.1UF 63V WIM MKS2MIN		C409
DG4148	DIODE 1N4148	REEL	D400-406 8
VA062	IC TL062CP	*STATIC	U403
VD4001BCN	IC CD4001BE	*STATIC	U401
VD4094BCN	IC CD4094BCN	*STATIC	U400
VD211CJ	IC DG211CJ	*STATIC	U402
VT328	BC328	TO-92D	Q400 2 4 6 8:10 2
VT212PL	BC212PL	E-LINE	Q401 3 5 7 9:11
TBM2510PS	10W 6410-22-27-2101		SK400
RAOMIT	RESISTORS OMITTED		R424 5
DAOMIT	DIODES OMITTED		D407
VS16L	IC SKT 703-1316-010410		U400 2
VS14L	IC SKT 703-1314-010410		U401
VS8P	IC SKT 703-1308-010410		U403
RM15R1025	5R1 1% MRS25	REEL	R403:11 5 9:23
RM210R025	10R 1% MRS25	REEL	R438
RLINK24	24 SWG TC LINK		R407
CE233U0IFC	33UF 35V KMVBFC 5 PITC		C407 8
CE210U0KFC	10UF 50V KMVBFC 5 PITC		C400-405
RM210R025	10R 1% MRS25	REEL	R31:52
RM218R025	18R 1% MRS25	REEL	R43
RM222R025	22R 1% MUL MRS25		R34:40 8:56
RM233R025	33R 1% MUL MRS25		R25:37:53 9:61
RM247R025	47R 1% MRS25	REEL	R6:41:60
RM251R025	51R 1% MUL MRS25		R26:49
RM3100R25	100R 1% MRS25	REEL	R1 3 5 7 8:27:44:57:63
RM3180R25	180R 1% MUL MRS25		R4
RM3270R25	270R 1% MRS25	REEL	R2
RM41K2025	1K2R 1% MRS25	REEL	R15-19:54:62
RM42K7025	2K7R 1% MRS25	REEL	R32 8:46:64 5 8:70
RM43K9025	3K9R 1% MUL MRS25		R28:33 9:47:55
RM45K6025	5K6R 1% MUL MRS25		R30 6:42:51 8:72

MAIN UNIT ITEM NUMBER : 17PSG1000 DESCRIPTION : TEL/N *PSG1000 *0050

FARNELL PART NUMBER	DESCRIPTION		CIRCUIT REFERENCE
RM510K025	10KR 1% MRS25	REEL	R11:66
RM515K025	15KR 1% MRS25	REEL	R12 3
RM527K025	27KR 1% MRS25	REEL	R67
RM533K025	33KR 1% MUL MRS25		R14
RM547K025	47KR 1% MRS25	REEL	R20-24:69
RM568K025	68KR 1% MRS25	REEL	R10
RM6120K25	120K 1% MRS25	REEL	R9
CC247P0N642	47PF 100V 683-34479		C24:35
CC3470PN630	470PF 100V 630-18471		C2-7:10-12 4 5 17-20 2 3 25-27 29-31 3 4 36-40 8
CC44K70N630	4K7PF 100V 630-19472		C16:21 8:32
CD41K751214	F/CAP 1K75PF ERI 1214		C42-44
DG221	DIODE BB221 ITT		D1 3:11 2
DG284	DIODE BA284		D2 5:10 3 6:22 3 6
DG329	DIODE BB329		D4 6-9:14 5:24 5
DG479	DIODE BA479 AEG ONLY		D17-20
DG4148	DIODE 1N4148	REEL	D21
VA0M350	HYBRID AMP 0M350		U1 2:12
VA061	IC TL061CP	*STATIC	U3
VA3199E	INT CCT CA3199E RCA		U7-10
VD4001BCN	IC CD4001BE	*STATIC	U11
VD212CJ	IC DG212CJ	*STATIC	U4
VD4094BCN	IC CD4094BCN	*STATIC	U5
VA822BS	IC U822BS	*STATIC	U6
VT328	BC328	TO-92D	Q1 3-6
VTR90A	TRANS BFR90A/02 L/NOIS		Q2
VT212PL	BC212PL	E-LINE	Q7
ZC0290	3SR/B *YE315S 4 TURNS		L1 2:13 4
T8M2503P0	3W 4030 22-03-2031		SK1
TL2W	2W TERM LINK 15-38 102		S1:500
VS8P	IC SKT 703-1308-010410		U3
VS14L	IC SKT 703-1314-010410		U11
VS16L	IC SKT 703-1316-010410		U4 5
RM3470R25	470R 1% MRS25	REEL	R29:71
BC1037	C /D *RANGE DIV *7RBT		B
CF41K50NFKS2	1K5PF 100V WIM FKS2		C41
ZZ9F30132	3 /B *CHK R/DIV PSG		L4 5 6
ZZ9F30133	3 /B *CHK R/DIV PSG		L7 8
ZZ9F30134	3 /B *CHK R/DIV PSG		L9:10
ZZ9F30136	3 /B *CHK R/DIV PSG		L11 2
ZC0291	3SR/C *YE315S 1 TURN		L15
CC3100PN642	100PF 100V 683-34101		C45
PM6100K67T	100K TYPE 67T		P1
PM550K067T	50KR TYPE 67T		P2
YT18	T/C WIRE 18SWG		L3
CC210P0N642	10PF 100V 683-10109		C46
CC12P20N642	2P2F 100V 683-09228		C47
CC14P70N642	4P7F 100V 683-09478		C49:50
CC12P70N642	2P7F 100V 683-09278		C8:51
RM3220R25	220R 1% MUL MRS25		R50
CE233U0IFC	33UF 35V KMVBFC 5 PITC		C1 9
CD41K751214	F/CAP 1K75PF ERI 1214		C600-613
ZC0291	3SR/C *YE315S 1 TURN		L600-606
5NPSG1000UHF			CCT BOARD: CPS/D *UHF CB ASSY
RM43K3025	3K3R 1% MRS25	REEL	R05
VTR90A	TRANS BFR90A/02 L/NOIS		Q01
DG221	DIODE BB221 ITT		D01 2

MAIN UNIT ITEM NUMBER : 17PSG1000 DESCRIPTION : TEL/N *PSG1000 *0050

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
CE247U0FD	47UF 16V DUB K	C04
BC1036	3 /B *UHF OSC *7SKK	B
ZC0290	3SR/B *YE315S 4 TURNS	L02
RM268R025	68R 1% MUL MRS25	R07
RM282R025	82R 1% MRS25 REEL	R06
RM3270R25	270R 1% MRS25 REEL	R01 4
CD41K751214	F/CAP 1K75PF ERI 1214	C206-208
ZC15U10	CHOKE 15UH SC10 ITT	L01 3
RM527K025	27KR 1% MRS25 REEL	R08
CC247P0682	47PF 100V 682 34479	C3
4NPSG1000SB		ASSEMBLY: SUB/B *SYNTHESIZER BOX
5NPSG1000HS		CCT BOARD: CPS/C *HF SYNTHESIZER
5NPSG1000HS1		CCT BOARD: CPS/B *HF SYNTH COMPS
RM210R025	10R 1% MRS25 REEL	R101
RM222R025	22R 1% MUL MRS25	R109
RM41K0025	1K0R 1% MRS25 REEL	R102 4 5
RM41K5025	1K5R 1% MRS25 REEL	R108
RM510K025	10KR 1% MRS25 REEL	R103:10
CC44K70N630	4K7PF 100V 630-19472	C101 2 5
CD41K751214	F/CAP 1K75PF ERI 1214	C109
CE233U0IEK	33UF 35V KMVB ECC	C103
CE247U0DFC	47UF 10V KMVB 5 PITCH	C104
CF510K0N2MIN	10KPF 100V 20% FKS2MIN	C107
DG284	DIODE BA284	D101 2
PM510K064W	10K SPL 64W	P101
VD74HC390N	IC 74HC390N *STATIC	U101
VD74HC00N	IC 74HC00N *STATIC	U102
VTX313	ZTX313 E-LINE	Q101
VX0386	CRYSTAL TCX04-B0386	XTL1
VS14L	IC SKT 703-1314-010410	U102
VS16L	IC SKT 703-1316-010410	U101
SR161A	REED RELAY 161-1	RL101
DG4148	DIODE 1N4148 REEL	D103
CC41K00N630	1K0PF 100 630-19102	C106
RM3330R25	330R 1% MRS25 REEL	R106
CC256P0N642	56PF 100V 683-34569	C108
5NPSG1000HS2		CCT BOARD: CPS/E *HF SYNTH COMPS
RM251R025	51R 1% MUL MRS25	R212 4
RM3100R25	100R 1% MRS25 REEL	R213 5 8
RM3470R25	470R 1% MRS25 REEL	R220
RM41K0025	1K0R 1% MRS25 REEL	R216 9
RM49K1025	9K1R 1% MUL MRS25	R224
RM510K025	10KR 1% MRS25 REEL	R205-208:10:21
RM522K025	22KR 1% MUL MRS25	R204
RM543K025	43KR 1% MUL MRS25	R217
RM547K025	47KR 1% MRS25 REEL	R209
RM6100K25	100K 1% MRS25 REEL	R222 3 5
RC71M0025	1M0R 5% MUL CR25	R226
RC72M2025	2M2R 10% MUL CR25	R201 2
CC3470PN630	470PF 100V 630-18471	C210 3:20 1 5
CE233U0IEK	33UF 35V KMVB ECC	C214 9
CE247U0DFC	47UF 10V KMVB 5 PITCH	C206
CF0U100LMKS	0.1UF 63V WIM MKS2MIN	C208:15 8
CF11U00KMKS2	1UF 50V MKS2 20%	C217:23 4
CF510K0N2MIN	10KPF 100V 20% FKS2MIN	C207
DGD3F	DUAL ZDX3F FER	D201 2

MAIN UNIT ITEM NUMBER : 17PSG1000 DESCRIPTION : TEL/N *PSG1000 *0050

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
PM41K0063P	1KOR SPL 63P	P201
PM45K0063P	5KOR SPL 63P	P202 3
VD4013BE	IC CD4013BE *STATIC	U201
VD4071BCN	IC CD4071BCN *STATIC	U204
VD8629DP	INT CCT SP8629DP PLSY	U206
VD212CJ	IC DG212CJ *STATIC	U207:15
VA356TC	IC UAF356TC/LF356N	U208
VA062	IC TL062CP *STATIC	U209:10
VD4081BCN	IC CD4081BCN *STATIC	U213
VD8718DG	IC TYPE SP8718DG PLSY	U205
VD4069UBE	IC CD4069UBE *STATIC	U214
VD4094BCN	IC CD4094BCN *STATIC	U211
TBM2512PS	12W 6401 22-27 2121	SK201
TBM2503PO	3W 4030 22-03-2031	X201
TL2W	2W TERM LINK 15-38 102	LK1 2
VS8P	IC SKT 703-1308-010410	U205 6 8-10
VS14L	IC SKT 703-1314-010410	U201 4:13 4
VS16L	IC SKT 703-1316-010410	U202 7:11:25
VS20L	IC SKT 703-1320-010410	U203
VD7523JN	IC AD7523JN *STATIC	U212
VA8821DP	IC NJ8821DP	U203
VD74HC4094	IC M74HC4094 *STATIC	U202
CC3470PN6306	470PF 100V 630-19471	C201-205 9
RM6220K25	220K 1% MUL MRS25	R227
RM582K025	82KR 1% MRS25 REEL	R229
RM42K7025	2K7R 1% MRS25 REEL	R211
RM6120K25	120K 1% MRS25 REEL	R203:28
CF522K0L2MIN	22KPF 63V WIM MKS2MIN	C222
CF41K50NFKS2	1K5PF 100V WIM FKS2	C212
CC247P0N642	47PF 100V 683-34479	C211
DZ12V700W5	ZENER ZPD2.7 REEL	Z201
CA0MIT	CAPACITORS OMITTED	C216
RM527K025	27KR 1% MRS25 REEL	R230
CF0U470LMKS2	0.47UF 63V 10% MKS2	C227
CA50T	CAP SELECT ON TEST	C226
5NPSG1000HS3		CCT BOARD: CPS/D *HF SYNTH COMPS
RM247R025	47R 1% MRS25 REEL	R301
RM3100R25	100R 1% MRS25 REEL	R302 6
RM42K2025	2K2R 1% MRS25 REEL	R303
RM44K3025	4K3R 1% MUL MRS25	R305
RM44K7025	4K7R 1% MRS25 REEL	R304
CC210P0N642	10PF 100V 683-10109	C302 3
CC247P0N642	47PF 100V 683-34479	C301
CC3470PN630	470PF 100V 630-18471	C305
CD41K751214	F/CAP 1K75PF ERI 1214	C307 8
CE233U0IEK	33UF 35V KMVB ECC	C304 6
PM6100K63P	100KR SPL 63P	P301
VF310S	J310 SILICONIX *STATIC	Q301
ZC0292	3SR/A *YE315S 6 TURNS	L302
TBM2503PO	3W 4030 22-03-2031	X301
TL2W	2W TERM LINK 15-38 102	LK3
RM547K025	47KR 1% MRS25 REEL	R307
ZZ9F30130	3 /C *CHK SYNTH PSG	L301
DG809	DIODE BB809	D301 2
5NPSG1000HS4		CCT BOARD: CPS/A *HF SYNTH COMPS
RM3100R25	100R 1% MRS25 REEL	R402

MAIN UNIT ITEM NUMBER : 17PSG1000 DESCRIPTION : TEL/N *PSG1000 *0050

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
RM41K0025	1K0R 1% MRS25 REEL	R401
RM43K0025	3K0R 1% MUL MRS25	R409:10
CC3470PN630	470PF 100V 630-18471	C404 8
CC41K00N630	1K0PF 100 630-19102	C403:10
CD41K751214	F/CAP 1K75PF ERI 1214	C412 3
CE233U0IEK	33UF 35V KMVB ECC	C405 9
CF0U100LMKS	0.1UF 63V WIM MKS2MIN	C402:11
CASOT	CAP SELECT ON TEST	C401
DG45	DIODE BAV45	D401 2
PM6100K63P	100KR SPL 63P	P401
VA5534AN	INT CCT NE5534AN	U401
TBM2502P0	2W 4030-22-03-2021	X401 2
TL2W	2W TERM LINK 15-38 102	LK4 5
RM41K2025	1K2R 1% MRS25 REEL	R403 8
RM48K2025	8K2R 1% MRS25 REEL	R404-407
RM510K025	10KR 1% MRS25 REEL	R411
VP1A	TRANSITOR PAD TW1A	D401 2
CC3220PN683	220PF 100V 683-58221	C406 7
5NPSG10U0HS5		CCT BOARD: CPS/B *HF SYNTH COMPS
RM247R025	47R 1% MRS25 REEL	R501
RM251R025	51R 1% MUL MRS25	R504
RM268R025	68R 1% MUL MRS25	R506 8 9
RM3100R25	100R 1% MRS25 REEL	R505
RM3240R25	240R 1% MUL MRS25	R507
RM3360R25	360R 1% MUL MRS25	R503
RM49K1025	9K1R 1% MUL MRS25	R502
CC256P0N642	56PF 100V 683-34569	C507 9
CC282P0N642	82PF 100V 683-34829	C508
CC3470PN630	470PF 100V 630-18471	C502:10-15
CC41K00N630	1K0PF 100 630-19102	C504 6
CE247U0DFC	47UF 10V KMVB 5 PITCH	C501
CD41K751214	F/CAP 1K75PF ERI 1214	C516 7
CF0U220LMKS2	0.22U 63V MKS2 10%	C503 5
DZ16V200W5	ZPD6.2 ITT	Z501
VA1610C	INT CCT SL1610C	U502
VASBL1X	MIXER SBL1-X DALE	U503
VA0M350	HYBRID AMP 0M350	U504 5
ZC0290	3SR/B *YE315S 4 TURNS	L501 2
VS8P	IC SKT 703-1308-010410	U502
VS14L	IC SKT 703-1314-010410	U506-508
VS16L	IC SKT 703-1316-010410	U501
VD74F161APC	IC 74F161APC *STATIC	U501
ZC4U7	47NH 551-5172-05-0200	L503 4
5NPSG1000HS6		CCT BOARD: CPS/E *HF SYNTH COMPS
RM15R1025	5R1 1% MRS25 REEL	R611 4
RM222R025	22R 1% MUL MRS25	R627 9
RM239R025	39R 1% MUL MRS25	R628
RM251R025	51R 1% MUL MRS25	R624 5
RM3100R25	100R 1% MRS25 REEL	R610 2 3:23 6:30
RM3180R25	180R 1% MUL MRS25	R622
RM44K7025	4K7R 1% MRS25 REEL	R606 7
RM45K6025	5K6R 1% MUL MRS25	R602 9
RM510K025	10KR 1% MRS25 REEL	R601 5 8:19:31
CC3470PN630	470PF 100V 630-18471	C605 6 609-618
CC3680PN630	680PF 100V 630-19681	C607
CC41K00N630	1K0PF 100 630-19102	C608

MAIN UNIT ITEM NUMBER : 17PSG1000 DESCRIPTION : TEL/N *PSG1000 *0050

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
CD41K751214	F/CAP 1K75PF ERI 1214	C619-621
CE233U0IEK	33UF 35V KMVB ECC	C601 2
CF11U00KMKS2	1UF 50V MKS2 20%	C603:24
CF510K0N2MIN	10KPF 100V 20% FKS2MIN	C604
DG4148	DIODE 1N4148 REEL	D601 2 605-609
DGD3F	DUAL ZDX3F FER	D603 4
PM6100K63P	100KR SPL 63P	P601
VTR90A	TRANS BFR90A/02 L/NOIS	Q601
VD4011BE	IC CD4011BE *STATIC	U601
VA062	IC TL062CP *STATIC	U602
VA5534AN	INT CCT NE5534AN	U605
VA0M350	HYBRID AMP 0M350	U608
ZC0290	3SR/B *YE315S 4 TURNS	L601-603
TBM2503P0	3W 4030 22-03-2031	X601
TL2W	2W TERM LINK 15-38 102	LK71
VS8P	IC SKT 703-1308-010410	U602 5
VS14L	IC SKT 703-1314-010410	U601
VS16L	IC SKT 703-1316-010410	U603
VS20L	IC SKT 703-1320-010410	U604
VA8821DP	IC NJ8821DP	U604
VD8718DG	IC TYPE SP8718DG PLSY	U606
VA822BS	IC U822BS *STATIC	U607
RC71M0025	1MOR 5% MUL CR25	R603 4
VD74HC4094	IC M74HC4094 *STATIC	U603
RM42K7025	2K7R 1% MRS25 REEL	R620
CF0U470LMKS2	0.47UF 63V 10% MKS2	C622
CE247U0IEK	47UF 35V KMVB/ALT 50V	C623
RM41K0025	1KOR 1% MRS25 REEL	R618
RM46K8025	6K8R 1% MUL MRS25	R621
RM3470R25	470R 1% MRS25 REEL	R615
RM6220K25	220K 1% MUL MRS25	R616 7
CF0U220LMKS2	0.22U 63V MKS2 10%	C625
TBM2502P0	2W 4030-22-03-2021	X610
BC1040	C /C *SYNTHESIZR*7RBT	B
5NPSG1000HS7		CCT BOARD: CPS/A *HF SYNTH COMPS
BC1185	C /A *PSG F/DTEC*7D3K	B
RM3680R25	680R 1% MUL MRS25	R1 4 7-10
RM41K0025	1KOR 1% MRS25 REEL	R2 5
RM42K2025	2K2R 1% MRS25 REEL	R3 6
CF0U100LMKS	0.1UF 63V WIM MKS2MIN	C1
VA12040P	INT CCT MC12040P	U1
VS5468	SKT 702-5468-01-04-16	SK1 2
CD41K751214	F/CAP 1K75PF ERI 1214	C500-517
ZC0291	3SR/C *YE315S 1 TURN	L500-508
5NPSG1000UHF		CCT BOARD: CPS/D *UHF CB ASSY
RM43K3025	3K3R 1% MRS25 REEL	R05
VTR90A	TRANS BFR90A/02 L/NOIS	Q01
DG221	DIODE BB221 ITT	D01 2
CE247U0FD	47UF 16V DUB K	C04
BC1036	3 /B *UHF OSC *7SKK	B
ZC0290	3SR/B *YE315S 4 TURNS	L02
RM268R025	68R 1% MUL MRS25	R07
RM282R025	82R 1% MRS25 REEL	R06
RM3270R25	270R 1% MRS25 REEL	R01 4
CD41K751214	F/CAP 1K75PF ERI 1214	C206-208
ZC15U10	CHOKE 15UH SC10 ITT	L01 3

MAIN UNIT ITEM NUMBER : 17PSG1000 DESCRIPTION : TEL/N *PSG1000 *0050

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
RM527K025	27KR 1% MRS25 REEL	R03
CC247P0682	47PF 100V 682 34479	C3
RM6100K25	100K 1% MRS25 REEL	L1
CD3150PNC0G	150PF 100V DISC C0G	C1
RM15R1025	5R1 1% MRS25 REEL	R73:520-523
ZC0290	3SR/B *YE315S 4 TURNS	L16:308
47PSG10000A		ASSEMBLY: FIN/B *O/P AMP/ATTEN
5NPSG10000A		CCT BOARD: CPS/F *OUTPUT AMP CB
BC1038	3 /B *OP AMP ATN*7DKK	B
RM3470R25	470R 1% MRS25 REEL	R18
RM41K5025	1K5R 1% MRS25 REEL	R4
RM41K8025	1K8R 1% MUL MRS25	R17
RM42K7025	2K7R 1% MRS25 REEL	R8 9
RM43K3025	3K3R 1% MRS25 REEL	R10
RM43K9025	3K9R 1% MUL MRS25	R7
RM44K7025	4K7R 1% MRS25 REEL	R1 5:42-44
RM45K6025	5K6R 1% MUL MRS25	R2 6:12
RM510K025	10KR 1% MRS25 REEL	R14
RM515K025	15KR 1% MRS25 REEL	R3
RM539K025	39KR 1% MUL MRS25	R13
RM547K025	47KR 1% MRS25 REEL	R15 6
RM6100K25	100K 1% MRS25 REEL	R11
CC12P20682	2P2F 100V 682	C3
CC247P0682	47PF 100V 682 34479	C2:10
CC282P0682	82PF 100V 682 34829	C6 7
CC3470PN630	470PF 100V 630-18471	C1 4 5 8
CD41K751214	F/CAP 1K75PF ERI 1214	C12-34
DG479	DIODE BA479 AEG ONLY	D1-3
DG4148	DIODE 1N4148 REEL	D4 5
DG2826	DIODE 5082-2826	D6 7
DG62	DIODE BAW62	D8-11
PM3500R67	500R SPL M67 SERIES	P2
ZC0290	3SR/B *YE315S 4 TURNS	L1
ZC0292	3SR/A *YE315S 6 TURNS	L2
VT212PL	BC212PL E-LINE	Q1
VT182PL	BC182PL E-LINE	Q2
VA061	IC TL061CP *STATIC	U1
VAOM370	AMPLIFIER OM370	U2
SR1725	RELAY 172-5	RL1-7
DZ15V601W3A	BZV85C5V6 MUL	D12 3
RM222R025	22R 1% MUL MRS25	R20
CAOMIT	CAPACITORS OMITTED	C11
RM15R1025	5R1 1% MRS25 REEL	R41
ZC0U510	CHOKE 0U5H SC10 0U47H	L3-5
RM3330R25	330R 1% MRS25 REEL	R45
RM3360R25	360R 1% MUL MRS25	R46
CC11P80N632	1P8F 100V 632	C36 7
CC210P0N642	10PF 100V 683-10109	C39
CC222P0N642	22PF 100V 683-34229	C38
RM268R025	68R 1% MUL MRS25	R19
PM6100K67T	100K TYPE 67T	P1
TBM2512HP	12W 6471 22 01 2125	S1 4:103:201:301
TBM2510HP	10W 6471-1 22-01 2105	S3:400
TBM2516HP	16W 6471-22-01-2165	S302
TBM3906HS	6W 2139-09-50-3061	S2
TBM3902HS	2W 2139 09-50-3021	S2

MAIN UNIT ITEM NUMBER : 17PSG1000 DESCRIPTION : TEL/N *PSG1000 *0050

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
TBM2506HP	6W 6471-1-22-01-2065	S3
47PSG1000PS		ASSEMBLY: FIN/D *POWER SUPPLY
5NPSG1000PS		CCT BOARD: CPS/B *POWER SUPPLY
RM3680R25	680R 1% MUL MRS25	R4
RM41K0025	1KOR 1% MRS25 REEL	R5 6
RM43K9025	3K9R 1% MUL MRS25	R7:12
RM44K7025	4K7R 1% MRS25 REEL	R8:11
RM543K025	43KR 1% MUL MRS25	R13 4
RM547K025	47KR 1% MRS25 REEL	R9:10
RM6180K25	180K 1% MUL MRS25	R2
CE233U01EK	33UF 35V KMVB ECC	C12 5 7
CE247U0DFC	47UF 10V KMVB 5 PITCH	C5 7
CE41K00GE	1KUF 25V KMVB ECC	C13
CE42K20ITM	2K2UF 35V TSW NAT PAN	C9
CE44K70FTM	4K7UF 16V TSW TAG MNT	C1 2
CF0U100LMKS	0.1UF 63V WIM MKS2MIN	C8:10 1 4 6 8 9:22
CF0U220LMKS2	0.22U 63V MKS2 10%	C20 1
CF0U470LMKS2	0.47UF 63V 10% MKS2	C3 4 6
DG4148	DIODE 1N4148 REEL	D2-11
DG4003	DIODE 1N4003	D12
DBW02M	BRDG RECT W02M	BR1 2
PM41K0063P	1KOR SPL 63P	P1
PM71M0063P	1MOR SPL 63P	P2
VA337T	INT CCT LM337T NAT	U4
VF22	HEXFET IRFZ22	Q3 4
VT182PL	BC182PL E-LINE	Q1 2
TBM2510PS	10W 6410-22-27-2101	SK3
TBM3906PS	6W 2391 09 65 1061	SK2
BC1035	3 /B *PSG1000 PS*7DAA	B
DG3345	DIODE BYV33-45	D1
RM44K3025	4K3R 1% MUL MRS25	R3
RM6220K25	220K 1% MUL MRS25	R1
RM247R025	47R 1% MRS25 REEL	R15
RLINK24	24 SWG TC LINK	R18
RAOMIT	RESISTORS OMITTED	R18
TBM3910P0	10W 26-20-2101	SK1
TBM3905PS	5W 2391-09-65-1051	SK1
MC1	CERAMIC BEAD SDP1 MET	BR1 2 X1/L
DAOMIT	DIODES OMITTED	D13
VA2940CT5	IC LM2940CT5	U1 2
VA340AT12	IC LM340AT12 *STATIC	U3
SA35093RD	RED BUT 035093-001	SW1
SB5020	6W P/B PBMS5020 4A 250	SW1
SRHC4	RELAY HC4 12V DC	RL1
SRHC4B	RL BASE HC4 SS	RL1
FH2002	FUSE HOLDER L2002	F2
TR35004	JACK 50R 35004C24H BNC	SK1
TR30001	JACK CAP&CHAIN GE30001	SK1
ZR0306	2SR/E *PSG1000	TX1
TK212	SKT 3W RPC212P3S	SK4
RM44K7025	4K7R 1% MRS25 REEL	R16 7
5NPSG1000AX		CCT BOARD: CPS/A *AUXILLIARY CB
BC1094	3 /A *AUX PSG *7P3A	B
TBM2512PS	12W 6401 22-27 2121	S1
TBM2506PS	6W 6410-22-27-2061	S3
PM525K043P	25KR SPL 43P	P

MAIN UNIT ITEM NUMBER : 17PSG1000 DESCRIPTION : TEL/N *PSG1000 *0050

FARNELL PART NUMBER	DESCRIPTION		CIRCUIT REFERENCE
FT250M11	250MA A/S TDC11		F1
FT4A00S503	4AMP A/S S503		F2
TBM3915HS	15W 2139-09-50-3151		S1
27PSG1000CT			END ITEM: FIN/B *CONTROL CB ASM
5NPSG1000CT1			CCT BOARD: CPS/F *CONTROL SECTION
RM3470R25	470R 1% MRS25	REEL	R120
RM510K025	10KR 1% MRS25	REEL	R105 9:17 9:22 4
RM547K025	47KR 1% MRS25	REEL	R102 4:14 5 8
RM6470K25	470K 1% MUL MRS25		R103
RN510K0850	N/WORK 10K 850/91 SIL		N101 2
CE3100UIEK	100UF 35V KMVB ECC		C104
CF0U100LMKS	0.1UF 63V WIM MKS2MIN		C101-103 5 6 8 9:11-13
CF11U00KMKS2	1UF 50V MKS2 20%		C107:10
DG4148	DIODE 1N4148	REEL	D102-109
VT337	BC337	TO-92D	Q101 2
VT328	BC328	TO-92D	Q103 4
VD74HC374N	IC 74HC374N	*STATIC	U110-117
VD74HC00N	IC 74HC00N	*STATIC	U106
VD74HC138N	IC 74HC138N	*STATIC	U119:20
VD4040BCN	IC CD4040BCN/BE	*STATIC	U123
VD74HC02	IC 74HC02	*STATIC	U107 8
VD4013BE	IC CD4013BE	*STATIC	U126
VD4001P	IC HEF4001P	*STATIC	U109
VD4532P	IC HEF4532P	*STATIC	U127
VX4M00HC43U	CRYSTAL 4MHZ 5PPM HC43		XTL101
EA889	BUZZER 889/IS21A		W101
TIH2520NR1S	20W M52-1220-450 PYE		S101
TIH2526NR1S	26W HEAD M52-1226-450		S102
TBM2512PT	12W 4094 22 05 2125		S103
TBM2502P0	2W 4030-22-03-2021		S104
RM275R025	75R 1% MUL MRS25		R101 6-8:10-12
VD74HC240	IC MM74HC240	*STATIC	U121
VD74HC251	IC MM74HC251	*STATIC	U122
VD4078B	IC CD4078BE	*STATIC	U125
SS4023	DIL SWITCH SCS4023		SW10
DG4003	DIODE 1N4003		D101
VS40L	IC SKT 703-1340-010410		U124 8
VS40C	40W CARRIER 612-92-640		U105
VS28	IC SKT 28W 15-25-1285		U131
VS28C	28W CARRIER 612-92-628		U101-103
VS20L	IC SKT 703-1320-010410		U104:10 1 13-17:29:30
VS16L	IC SKT 703-1316-010410		U119:20 2 3 7
VD6264LP15	HM6264LP15	*STATIC	U103
VD27C128K	IC M5L27C128K	*STATIC	U102
VD80C85	IC MSM80C85A	*STATIC	U105
RM41K0025	1KOR 1% MRS25	REEL	R121
VA0MIT	TRANSISTORS/ICS OMITTE		U131 2:T101
VD74HCT373	IC 74HCT373	*STATIC	U104
VD8291A	IC P8291A	*STATIC	U128
VD75160AN	INT CCT SN75160AN		U129
VD75161AN	INT CCT SN75161AN		U130
RM44K7025	4K7R 1% MRS25	REEL	R123
CC233P0N642	33PF 100V 683-34339		C114 5
TL2W	2W TERM LINK 15-38 102		LK12-14
VD27C256	IC MMC27C256Q25	*STATIC	U101

MAIN UNIT ITEM NUMBER : 17PSG1000 DESCRIPTION : TEL/N *PSG1000 *0050

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
VD74HC08N	IC MM74HC08N *STATIC	U118
VD81C55	IC MSM81C55 *STATIC	U124
VS14L	IC SKT 703-1314-010410	U106-109:18:25 6
CASOT	CAP SELECT ON TEST	C116
VS28L	28W 703-1328-01-04-10	U131
5NPSG1000CT2		CCT BOARD: CPS/C *AUDIO SYNTH
RM522K025	22KR 1% MUL MRS25	R201 2
CC3150PN642	150PF 100V 683-34151	C208
CE233U0IEK	33UF 35V KMVB ECC	C201 2
CF41K50NFKS5	1K5PF 100V 5% WIM FKS2	C207
CF515K0LMKS2	15KPF 63V MKS2 10%	C206
VD4527	IC HEF4527BP *STATIC	U201-204
VD4013BE	IC CD4013BE *STATIC	U207
VD4011BE	IC CD4011BE *STATIC	U206
VA6CN50	INT CCT MF6CN-50	U210
VD212CJ	IC DG212CJ *STATIC	U211 2
VS16L	IC SKT 703-1316-010410	U201-205 8 9:11 2
VS14L	IC SKT 703-1314-010410	U206 7:10
VD14017BCP	IC MC14017BCP *STATIC	U205 8 9
CF0U100LMKS	0.1UF 63V WIM MKS2MIN	C209
RM516K025	16KR 1% MUL MRS25	R203
RM43K3025	3K3R 1% MRS25 REEL	R204
RM3180R25	180R 1% MUL MRS25	R207
CF11U00KMKS2	1UF 50V MKS2 20%	C210
VA79L05ACZ	INT CCT LM79L05ACZ	U213
CF533K0LMKS2	33KPF 63V WIM MKS2	C203
RASOT	**** SELECT ON TEST **	R206
RM539K025	39KR 1% MUL MRS25	R205
CF43K30NFKS2	3K3PF 100V WIM FKS2	C204
CC3330PN642	330PF 100V 683-58331	C205
PM525K063P	25KR SPL 63P	P201
EB1600	LD1600 0089-400-019	ISSUE DIRECT TO TEST
5NPSG1000CT3		CCT BOARD: CPS/D *MON CONTROL
RM247R025	47R 1% MRS25 REEL	R319:23
RM3470R25	470R 1% MRS25 REEL	R309:17
RM43K9025	3K9R 1% MUL MRS25	R305:29
RM510K025	10KR 1% MRS25 REEL	R306 7
RM512K025	12KR 1% MRS25 REEL	R325
RM515K025	15KR 1% MRS25 REEL	R314:24
RM522K025	22KR 1% MUL MRS25	R315
RM527K025	27KR 1% MRS25 REEL	R326
RM575K025	75KR 1% MRS25 REEL	R321
RM580K6251	80K6 1% MUL MRS25	R320
RM6100K25	100K 1% MRS25 REEL	R301:11
RM6220K25	220K 1% MUL MRS25	R308:18
RASOT	**** SELECT ON TEST **	R328
CE233U0IEK	33UF 35V KMVB ECC	C302 304-307:10 3
CF0U100LMKS	0.1UF 63V WIM MKS2MIN	C303 8:16-18
CF11U00KMKS2	1UF 50V MKS2 20%	C301
CF41K50NFKS5	1K5PF 100V 5% WIM FKS2	C311 2
CP42K00HFSC	2K0PF 30V FSC/TP 1%	C309
DZ16V200W4	IN823 MOT	D301
PM510K063P	10KR SPL 63P	P303 5
PM525K063P	25KR SPL 63P	P302 6
PM6100K63P	100KR SPL 63P	P301 4
VD4011BE	IC CD4011BE *STATIC	U313

MAIN UNIT ITEM NUMBER : 17PSG1000 DESCRIPTION : TEL/N *PSG1000 *0050

FARNELL PART NUMBER	DESCRIPTION		CIRCUIT REFERENCE
VD4069UBE	IC CD4069UBE	*STATIC	U314
VD212CJ	IC DG212CJ	*STATIC	U301 3 4
VD4013BE	IC CD4013BE	*STATIC	U308
VA062	IC TL062CP	*STATIC	U302 5
VA353N	IC LF353N	*STATIC	U307
TBM2512PT	12W 4094 22 05 2125		S301
T3M2516PT	16W 4094-22-05-2161		S302
VD7530JN	IC AD7530JN	*STATIC	U306:15
VA6CN100	IC MF6CN100	*STATIC	U312
VS16L	IC SKT 703-1316-010410		U301 3 4 6 9:10 1 5
VS14L	IC SKT 703-1314-010410		U303:12-14
VS8P	IC SKT 703-1308-010410		U302 5 7:16
VD14017BCP	IC MC14017BCP	*STATIC	U309-311
RM42K2025	2K2R 1% MRS25	REEL	R312
RM533K025	33KR 1% MUL MRS25		R316
RM518K025	18KR 1% MRS25	REEL	R310:27
RM3180R25	180R 1% MUL MRS25		R330
RM524K025	24KR 1% MRS25	REEL	R313
RM44K7025	4K7R 1% MRS25	REEL	R322:31
RM6150K25	150K 1% MRS25	REEL	R302 4
RA0MIT	RESISTORS OMITTED		R303
CC15P60N642	5P6F 100V 683-09568		C314
CC247P0N642	47PF 100V 683-34479		C315
VA79L05ACZ	INT CCT LM79L05ACZ		U317
VA061	IC TL061CP	*STATIC	U316
VA0MIT	TRANSISTORS/ICS OMITTE		U131 2:T101
5NPSG1000CT4			CCT BOARD: CPS/D *SINAD +METR DRV
RM41K0025	1K0R 1% MRS25	REEL	R416:23 4:32 9
RM42K0025	2K0R 1% MUL MRS25		R427:30
RM42K7025	2K7R 1% MRS25	REEL	R405
RM45K6025	5K6R 1% MUL MRS25		R411
RM510K025	10KR 1% MRS25	REEL	R401 4 8:12
RM522K025	22KR 1% MUL MRS25		R436
RM547K025	47KR 1% MRS25	REEL	R406
RM6100K25	100K 1% MRS25	REEL	R418-422 6 8 9:31 4
RM6200K25	200K 1% MUL MRS25		R409:10
RM6270K25	270K 1% MUL MRS25		R417
RM6470K25	470K 1% MUL MRS25		R415:25:33
RC71M0025	1M0R 5% MUL CR25		R403
CC215P0N642	15PF 100V 683-10159		C412 6 7
CE210U0KE	10UF 50V KMV8		C403 5 6 8
CE233U0IEK	33UF 35V KMV8 ECC		C409:10 4 5
CF0U100LMKS	0.1UF 63V WIM MKS2MIN		C411
CF11U00KMKS2	1UF 50V MKS2 20%		C401:18
CF41K50NFKS2	1K5PF 100V WIM FKS2		C407
DG4148	DIODE 1N4148	REEL	D401-405
PM3500R63P	500R SPL 63P		P407
PM45K0063P	5K0R SPL 63P		P402
PM510K063P	10KR SPL 63P		P401
PM6100K63P	100KR SPL 63P		P404-406
PM71M0063P	1M0R SPL 63P		P403
VA062	IC TL062CP	*STATIC	U403
VA061	IC TL061CP	*STATIC	U407
VA3046	VT ARRAY CA3046 RCA		U406
VD211CJ	IC DG211CJ	*STATIC	U405
VA064CN	IC TL064CN	*STATIC	U404

MAIN UNIT ITEM NUMBER : 17PSG1000 DESCRIPTION : TEL/N *PSG1000 *0050

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
VA6270CDP	INT CCT SL6270CDP	U401
VA10CN	IC MF10CN *STATIC	U402
VS20L	IC SKT 703-1320-010410	U402
VS16L	IC SKT 703-1316-010410	U405
VS14L	IC SKT 703-1314-010410	U404 6
VS8P	IC SKT 703-1308-010410	U401 3 7
RASOT	**** SELECT ON TEST **	R413
RM44K7025	4K7R 1% MRS25 REEL	R407
RM511K025	11KR 1% MUL MRS25	R437
RM3100R25	100R 1% MRS25 REEL	R435
CC3100PN642	100PF 100V 683-34101	C413
CE3100UCD	100UF 6.3V DUB K1006	C404
RM247R025	47R 1% MRS25 REEL	R404
RM6150K25	150K 1% MRS25 REEL	R414
BC1039	C /C *CONTROL C9*7RBT	B

PSG1000 HARDWARE

FARNELL PART NUMBER	DESCRIPTION
CASING	
HA0065	HANDLE
HA0066	HANDLE INSERT
HF0067	MOULDED FOOT
HF0011	FOOT AND LEG ASM
HF0070	FOOT INSERT
7SU2438	TOP COVER
7SU2439	BOTTOM COVER
7SX2519	SIDE TRIM
HC22V2	MAINS LEAD
TR201A	BNC/N ADAPTER
HC0010	COAX LEAD
HW3114003	EXTRACTOR
FRONT PANEL ASSEMBLY	
HKS111125BLK	KNOB
HK110	KNOB CAP
HK111	NUT COVER
HW0065	FRONT PANEL MEMBRANE
HW0101	TITLE INSERT (FRONT PANEL)
POWER SUPPLY ASM	
TG6J4	MAINS FILTER
RF BOX ASMS	
YMMNS513	RF GASKET
PRINTED CIRCUIT BOARDS	
BC1035	POWER SUPPLY
BC1036	UHF OSCILLATOR
BC1037	RANGE DIVIDER
BC1038	OUTPUT AMP
BC1039	CONTROL BOARD
BC1040	SYNTHESIZER
BC1041	DISPLAY TERMINAL
BC1094	AUXILIARY

P S G 1 0 0 0 M A N U A L

ADDENDUM

1. EXTERNAL BATTERY LEVEL INDICATION

The front panel battery level meter scale is calibrated with the pointer mid way between the red and black indication scales.

Indication accuracy at this point is 12V ± 1V for the standard unit and 24V ± 1V when the 23 to 30V option is fitted.

2. SEQUENTIAL TONE APPLICATIONS

To avoid false triggering of the radio tone decodes, the fixed audio frequency preceeding a selcall tone burst must not lie within the bands of allowable sequential tone frequencies.

SEQUENTIAL SYSTEMS						
	CCIR	EEA	ZVEI-1	ZVEI-2	EIA	NATEL
1	1124		1060	970	741	631
2	1197		1160	1060	882	697
3	1275		1270	1160	1023	770
4	1358		1400	1270	1164	852
5	1446		1530	1400	1305	941
6	1540		1670	1530	1446	1040
7	1640		1830	1670	1587	1209
8	1747		2000	1830	1728	1336
9	1860		2200	2000	1869	1477
0	1981		2400	2200	459	1633
Repeat	2110		2600	2400	600	1805
Tone Duration	100ms	40ms	70ms	70ms	33ms	70ms